

# 661FX-M

REV:1.0

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### Revision History :

1. Ver A: Initial
2. Ver 1.0: Change AUDIO1 header location

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**SIGNATURE**

**DATE**

**DESIGNER**


Jacy

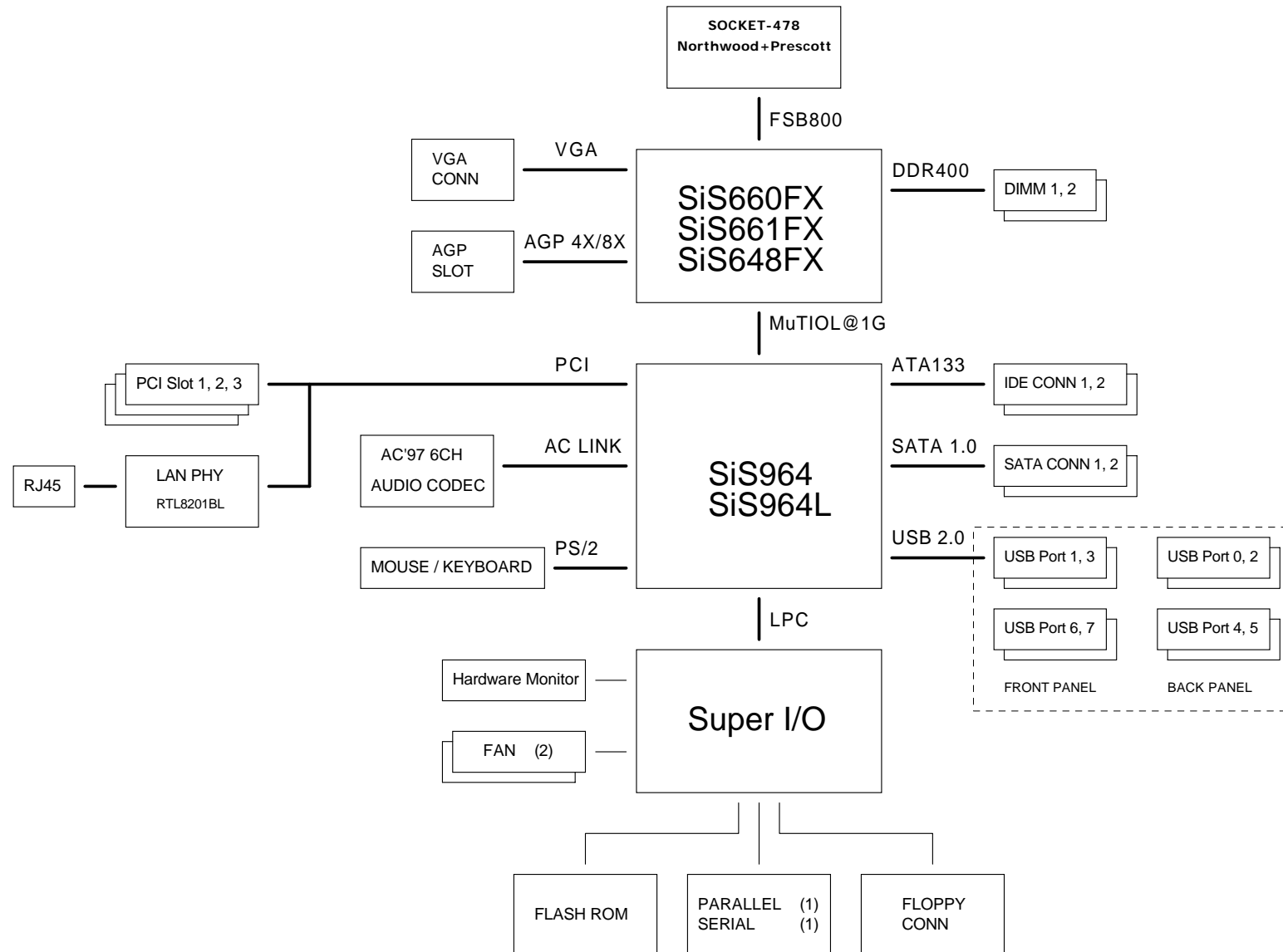
10/10/2003

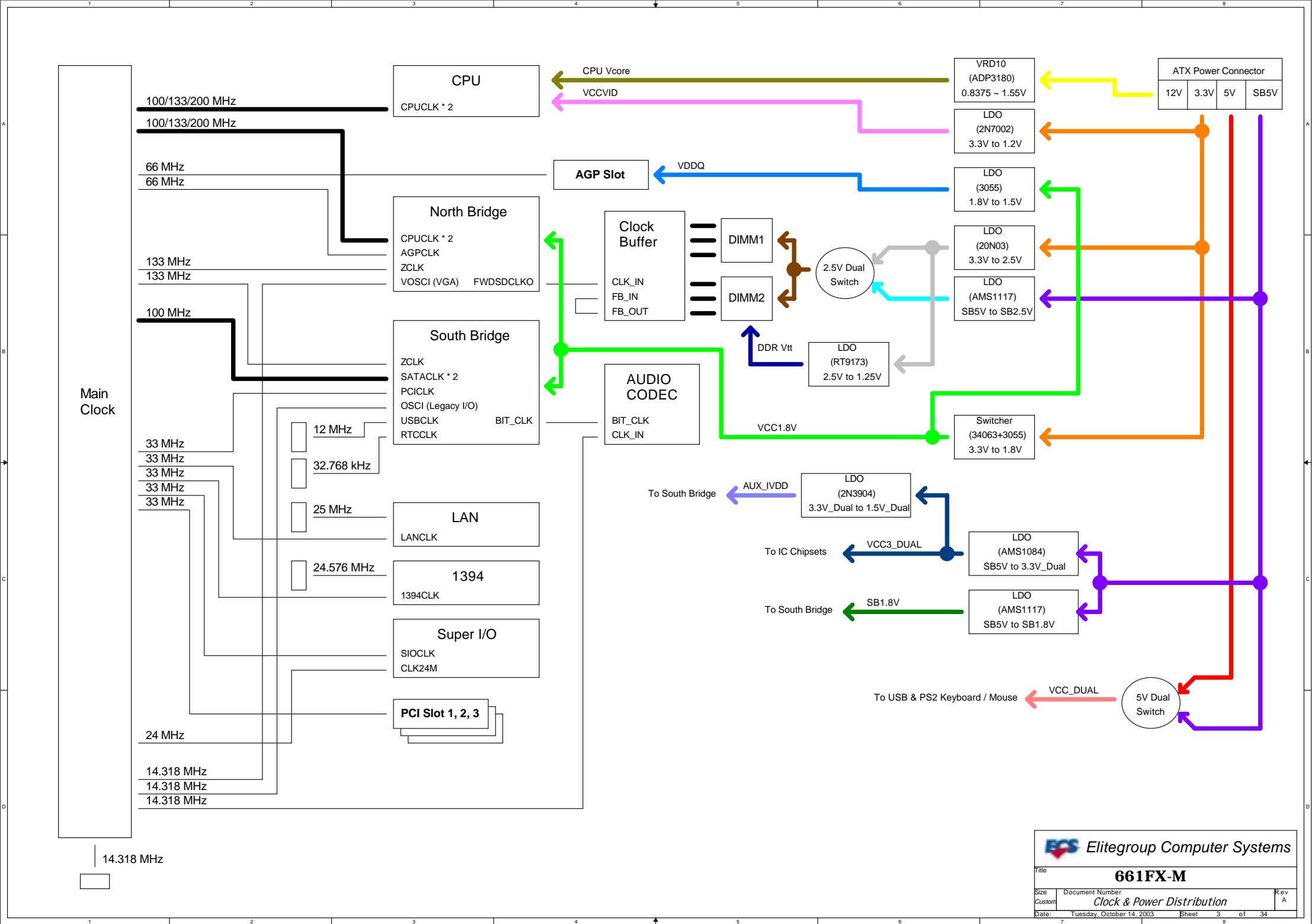
**LAYOUT**

**CHECK**

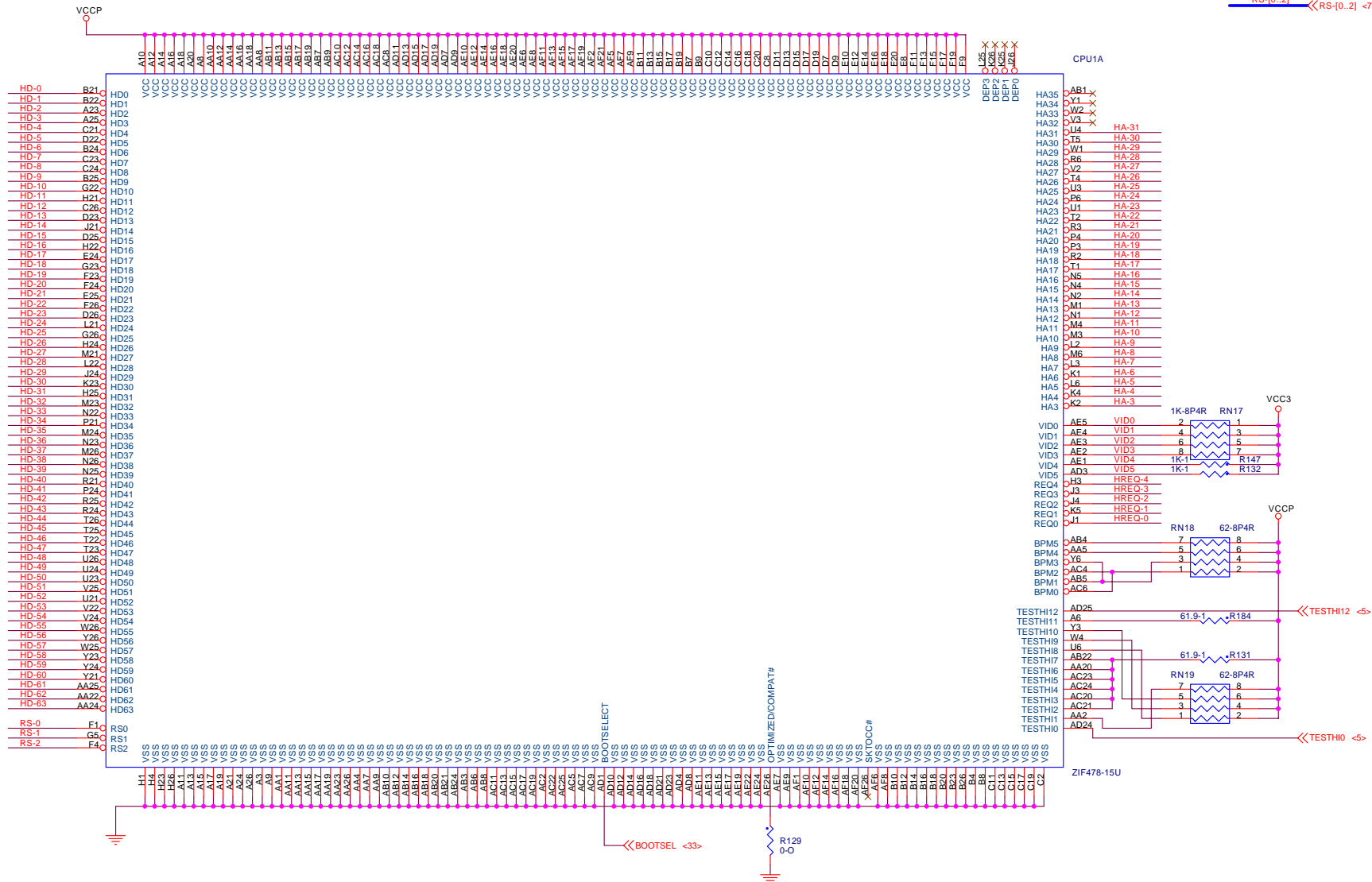
**APPROVAL**

 Elitegroup Computer Systems		
Title <b>661FX-M</b>		
Size	Document Number	Rev
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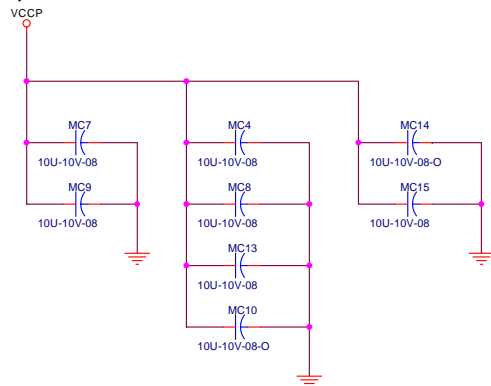


HD[0..63] <<HD-[0..63] <7>  
HA[3..31] <<HA-[3..31] <7>  
VID[0..5] <<VID[0..5] <33>  
HREQ[0..4] <<HREQ-[0..4] <7>  
RS[0..2] <<RS-[0..2] <7>

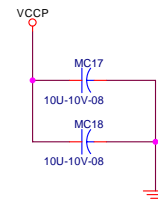




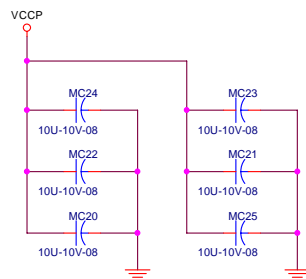
Put these capacitors at processor NORTH SIDE



Put these capacitors INSIDE PROCESSOR CAVITY

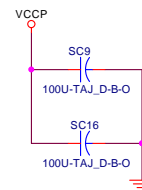


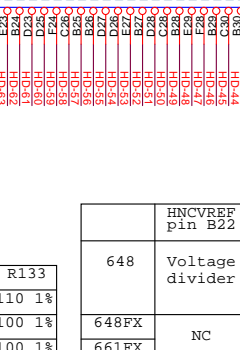
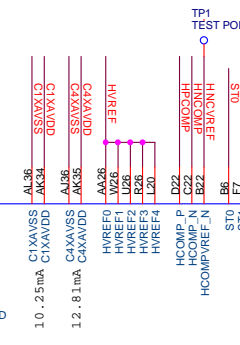
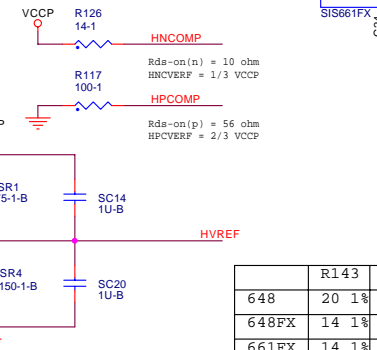
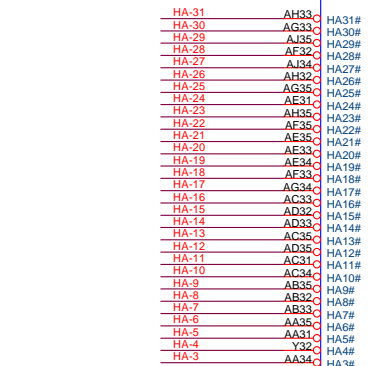
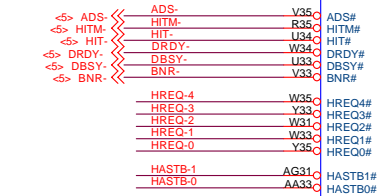
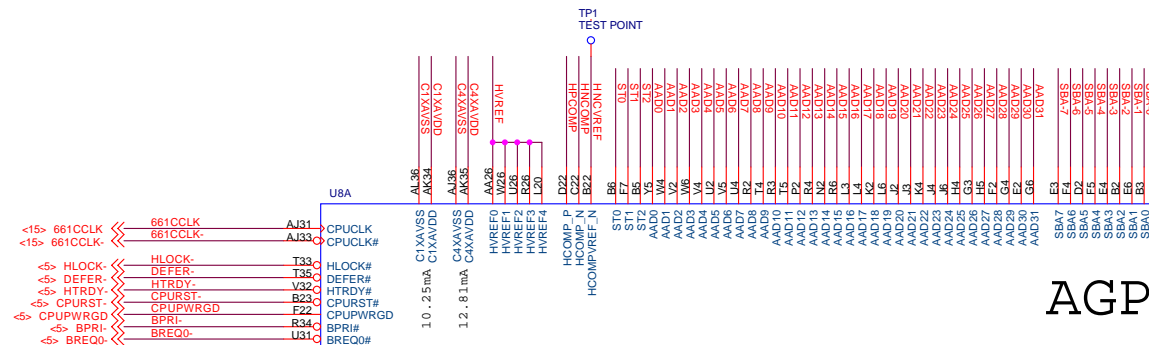
Put these capacitors at processor SOUTH SIDE

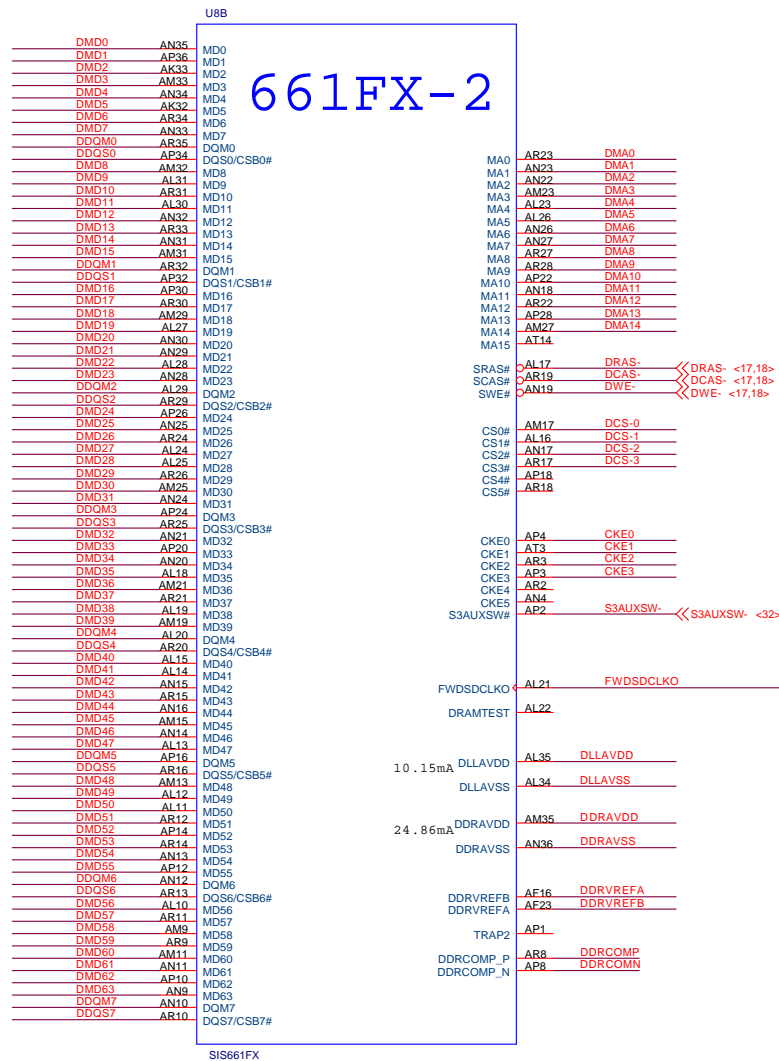


P.S. choose X7R/X5R components instead of Y5V for all 10uF\_1206 capacitors on this page.

Put these capacitors at processor SOLDER SIDE







DMD[0..63] <<DMD[0..63] <17,18>

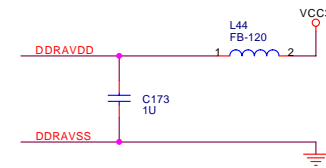
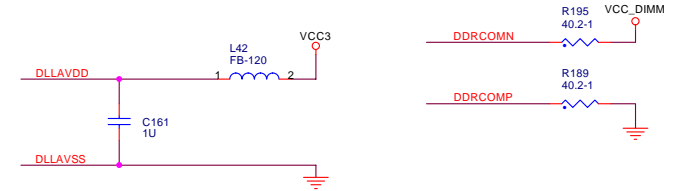
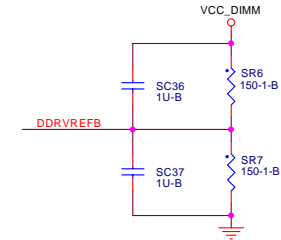
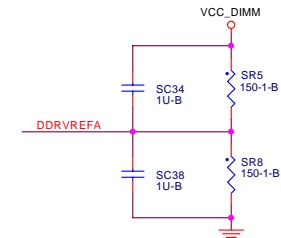
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DDQS[0..7] <<DDQS[0..7] <17,18>

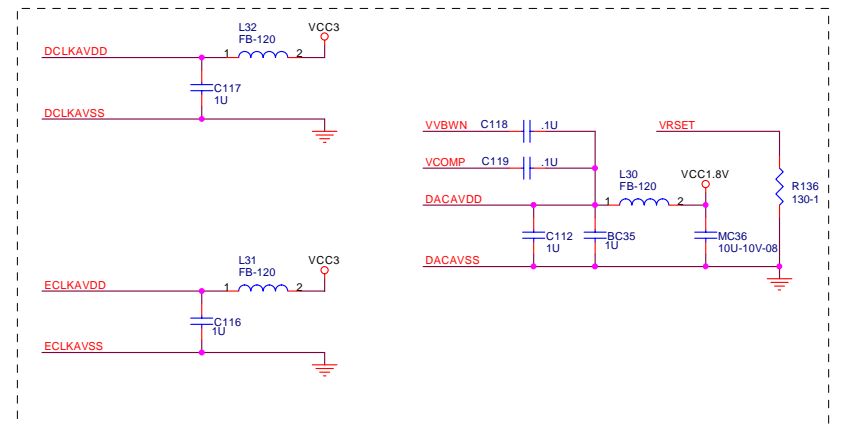
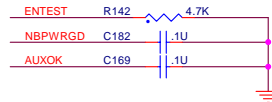
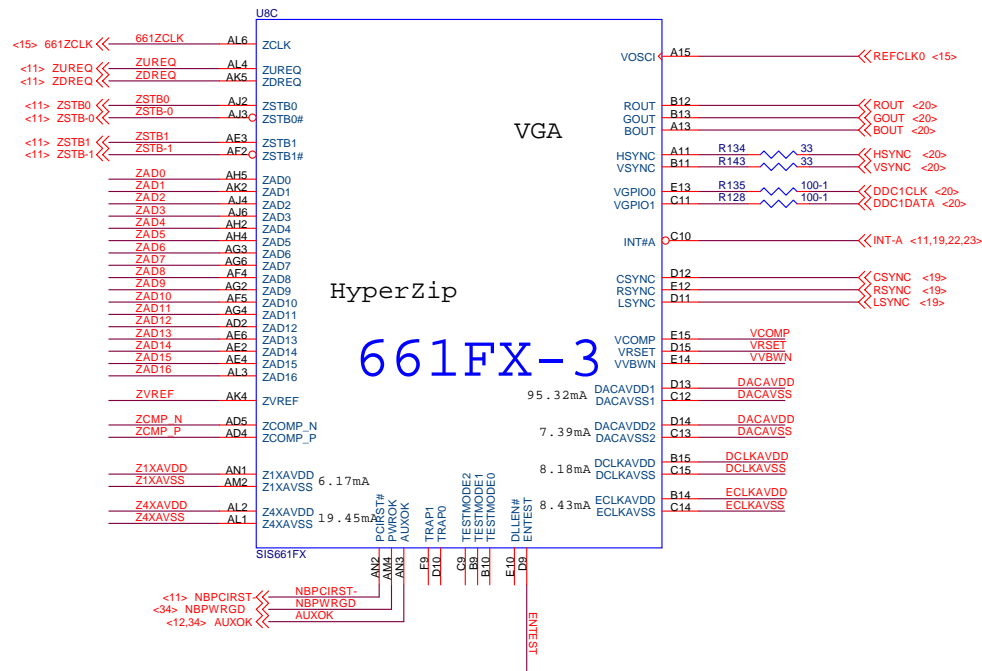
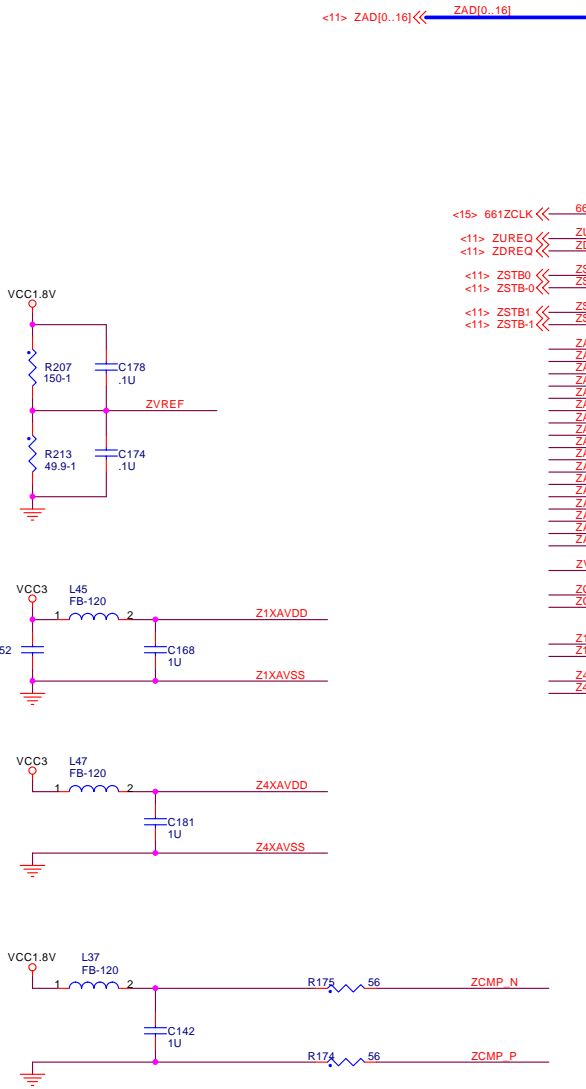
DMA[0..14] <<DMA[0..14] <17,18>

DCS-[0..3] <<DCS-[0..3] <17,18>

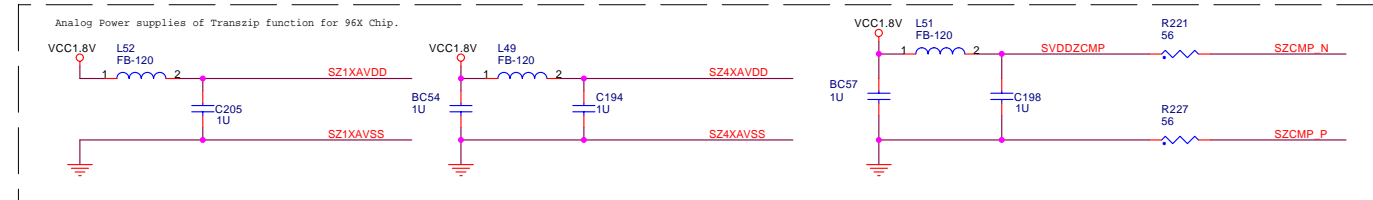
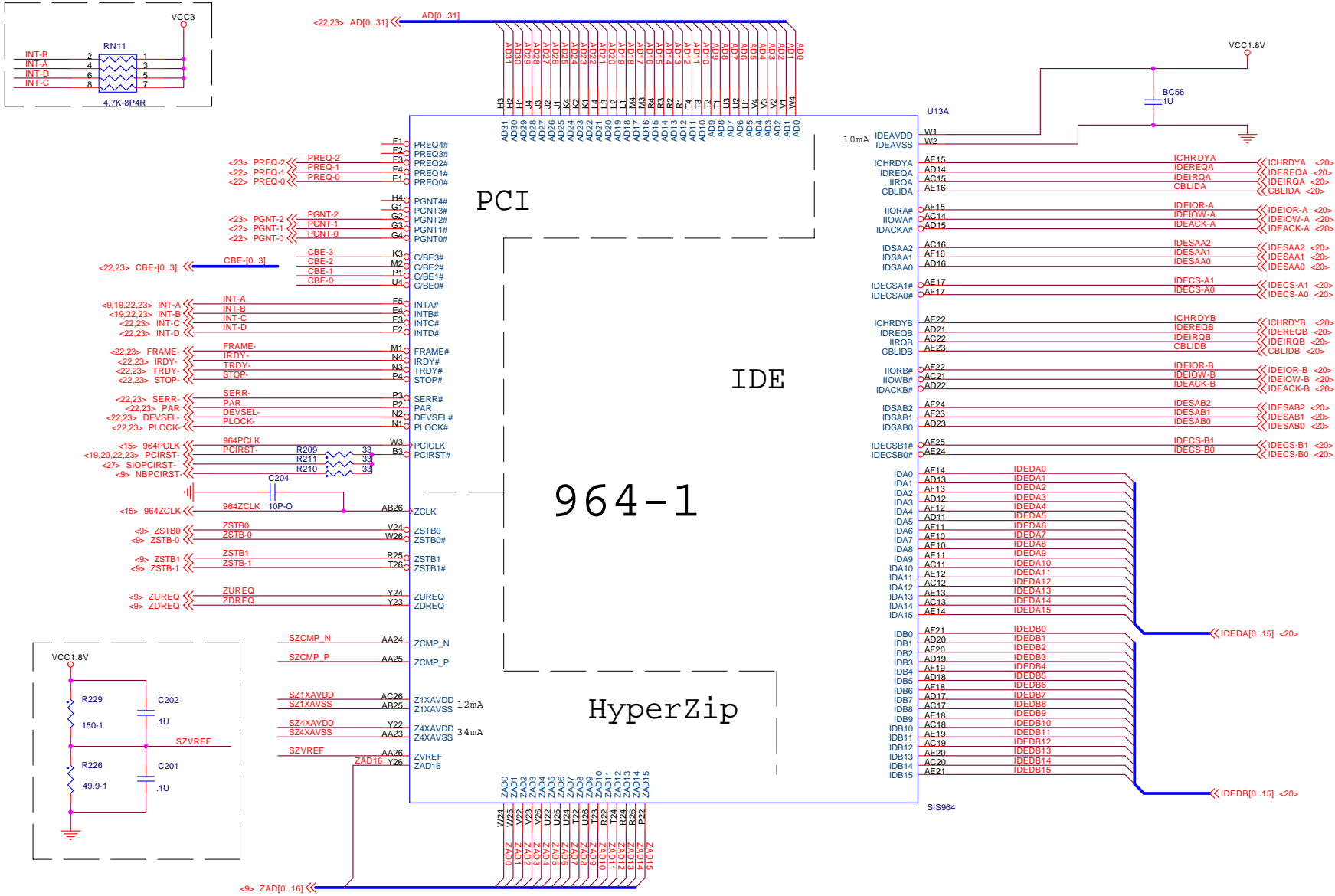
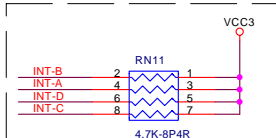
CKE[0..3] <<CKE[0..3] <17>



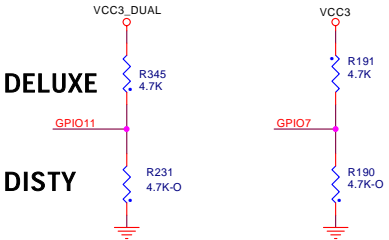
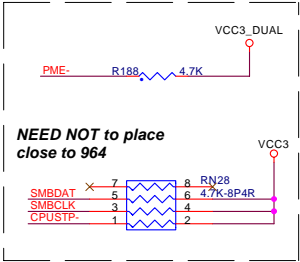
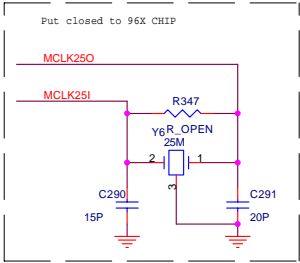
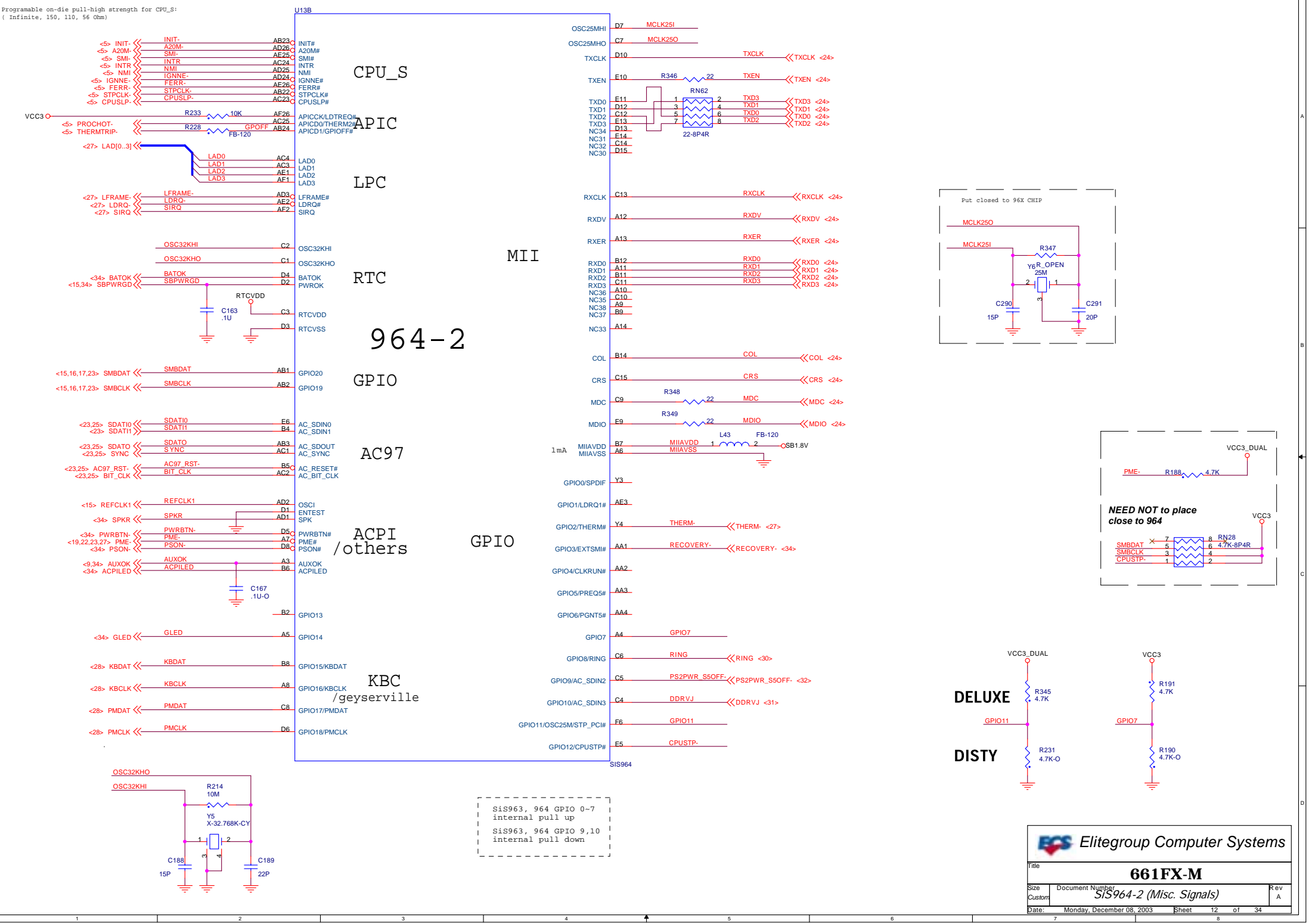


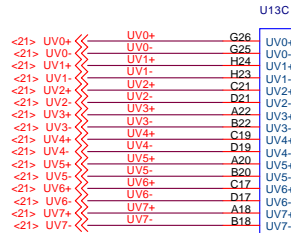
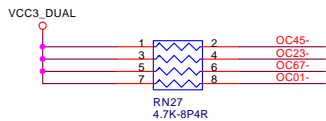






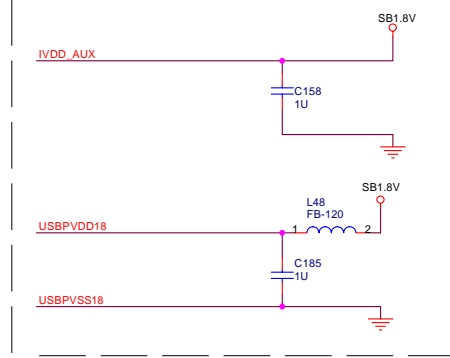
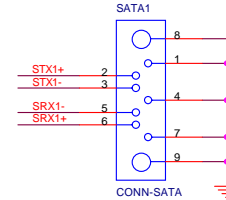
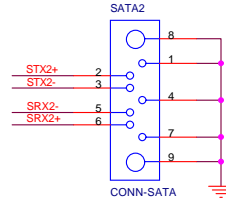
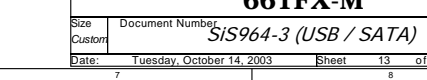
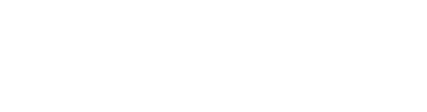
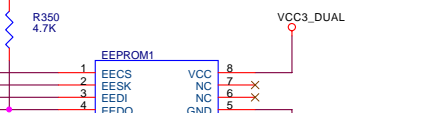
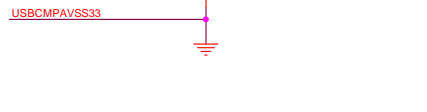
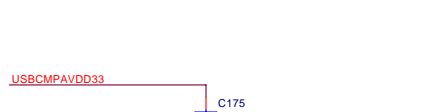
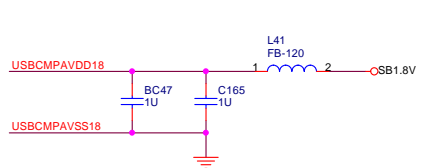
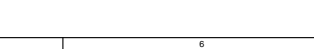
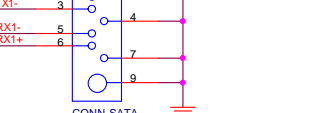
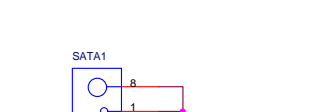
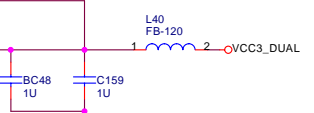
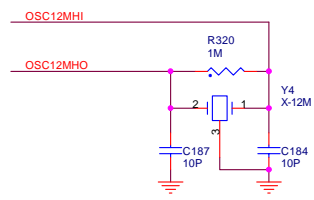
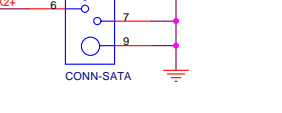
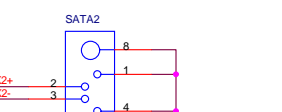
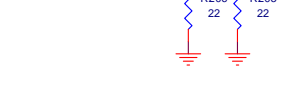
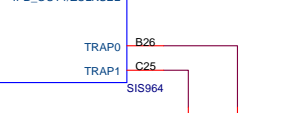
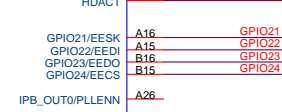
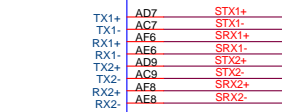
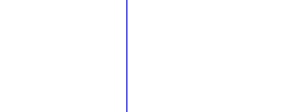
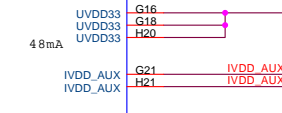
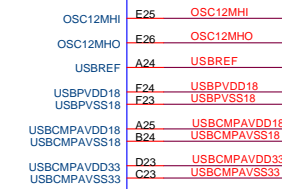
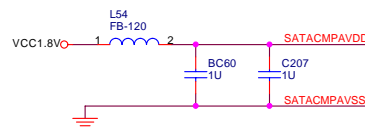
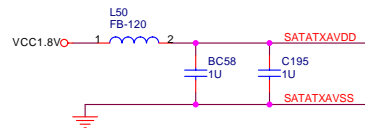
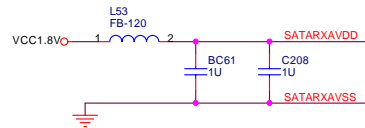
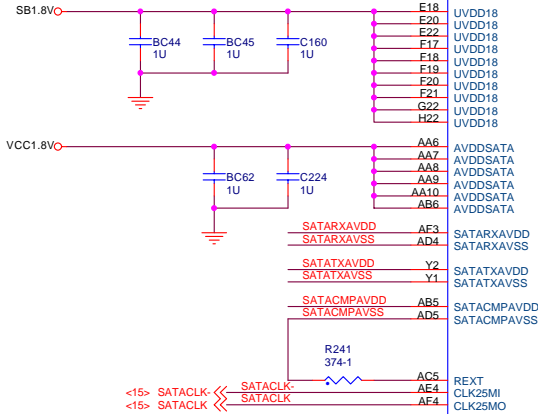
Programmable on-die pull-high strength for CPU\_S:  
( Infinite, 150, 110, 56 Ohm)





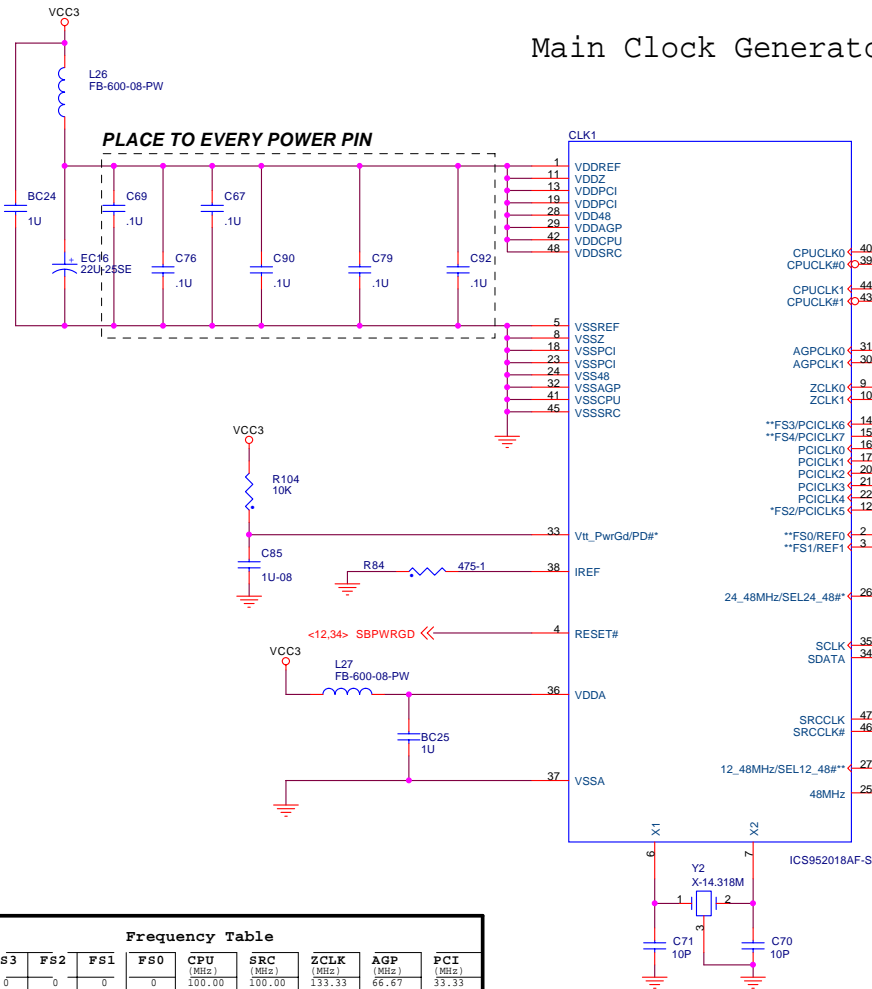
USB

964-3

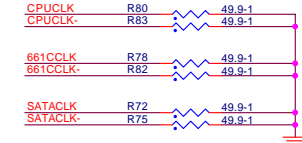




# Main Clock Generator



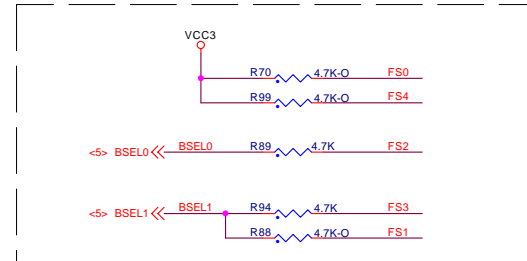
## By-Pass Capacitors Place near to the Clock Outputs



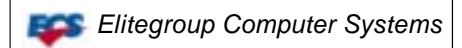
Frequency Table									
FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
0	0	0	0	0	100.00	100.00	133.33	66.67	33.33
0	0	0	0	1	100.99	100.99	134.65	67.33	33.66
0	0	0	1	0	103.00	103.00	137.33	68.67	34.33
0	0	1	0	0	100.00	100.00	133.33	66.67	33.33
0	0	1	0	1	133.33	100.00	133.33	66.66	33.33
0	0	1	1	0	134.65	100.99	134.65	67.32	33.66
0	0	1	1	1	137.33	103.00	137.33	68.66	34.33
0	1	0	0	0	133.33	100.00	133.33	66.67	33.33
0	1	0	0	1	200.00	100.00	133.33	66.67	33.33
0	1	0	1	0	201.98	100.99	134.65	67.33	33.66
0	1	0	1	1	206.00	103.00	137.33	68.67	34.33
0	1	1	0	0	200.00	100.00	133.33	66.67	33.33
0	1	1	0	1	166.66	125.00	125.00	66.66	33.33
0	1	1	1	0	168.31	126.23	126.23	67.32	33.66
0	1	1	1	1	171.66	128.74	128.74	68.66	34.33
0	1	1	1	1	166.66	125.00	125.00	66.66	33.33

Frequency Table									
FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
1	0	0	0	0	105.00	105.00	140.00	70.00	35.00
1	0	0	0	1	107.00	107.00	142.67	71.33	35.67
1	0	0	1	0	109.00	109.00	145.33	72.67	36.33
1	0	0	1	1	110.00	110.00	146.67	73.33	36.67
1	0	1	0	0	140.00	105.00	140.00	70.00	35.00
1	0	1	0	1	142.66	107.00	142.67	71.33	35.67
1	0	1	1	0	145.33	109.00	145.33	72.66	36.33
1	0	1	1	1	146.66	110.00	146.66	73.33	36.67
1	1	0	0	0	210.00	105.00	140.00	70.00	35.00
1	1	0	0	1	214.00	107.00	142.67	71.33	35.67
1	1	0	1	0	218.00	109.00	145.33	72.67	36.33
1	1	0	1	1	220.00	110.00	146.67	73.33	36.67
1	1	1	0	0	266.66	100.00	133.33	66.67	33.33
1	1	1	0	1	269.33	101.00	134.67	67.33	33.67
1	1	1	1	0	274.66	103.00	137.33	68.67	34.33
1	1	1	1	1	266.66	100.00	133.33	66.67	33.33

## Frequency Selection



Clock Generator Table					
Hardware Trapping					
CPU=100 (BSEL[1:0]=00)	FS4	FS3	FS2	FS1	FS0
	Low	BSEL1	BSEL0	Low	Low
CPU=133 (BSEL[1:0]=01)	0	0	1	0	0
CPU=200 (BSEL[1:0]=10)	0	1	0	0	0

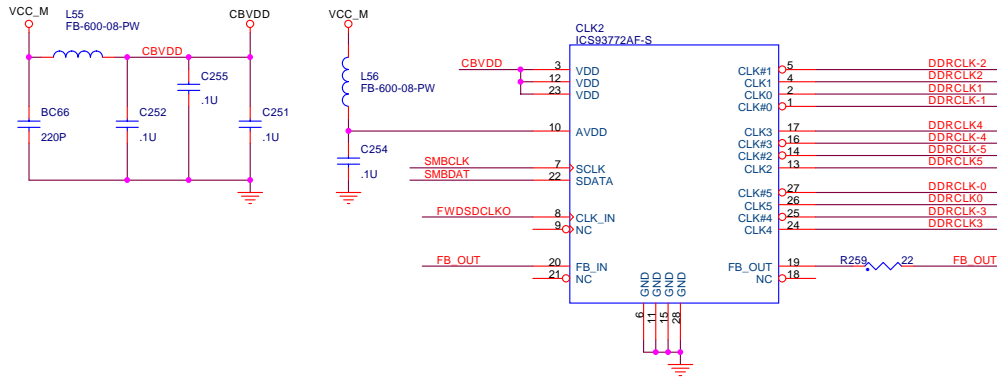


661FX-M				
Title	Document Number	Main Clock		Rev A
Size	Custom	Main Clock		Rev A
Date:	Tuesday, October 14, 2003	Sheet	15	of 34

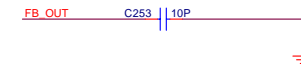
## Clock Buffer (DDR)

(5 OPTIONS)  
 1: (ICS) ICS93716  
 2: (Winbond)  
 3: (ICWorks)  
 4: (IMI)  
 5: (AMI)

By-Pass Capacitors  
 Place near to the Clock Buffer



DDRCLK[0..5] <<DDRCLK[0..5] <17>  
 DDRCLK[0..5] <<DDRCLK[0..5] <17>  
 SMBCLK <<SMBCLK <12,15,17,23>  
 SMBDAT <<SMBDAT <12,15,17,23>  
 FWSDCLKO <<FWSDCLKO <8>



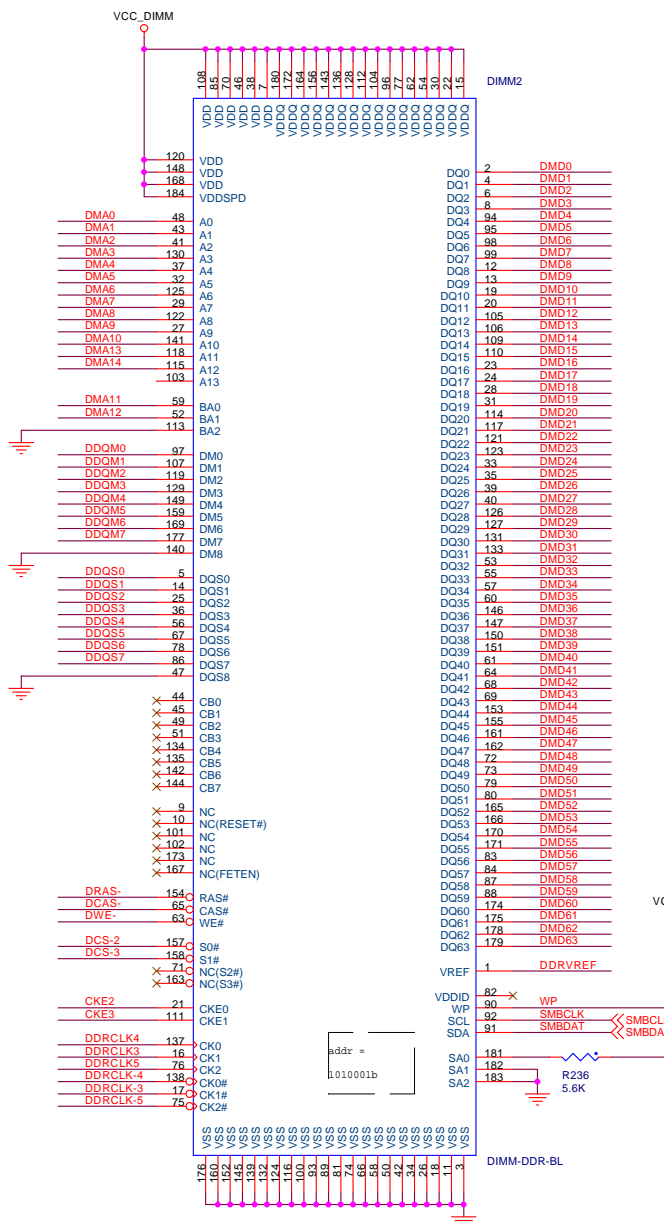
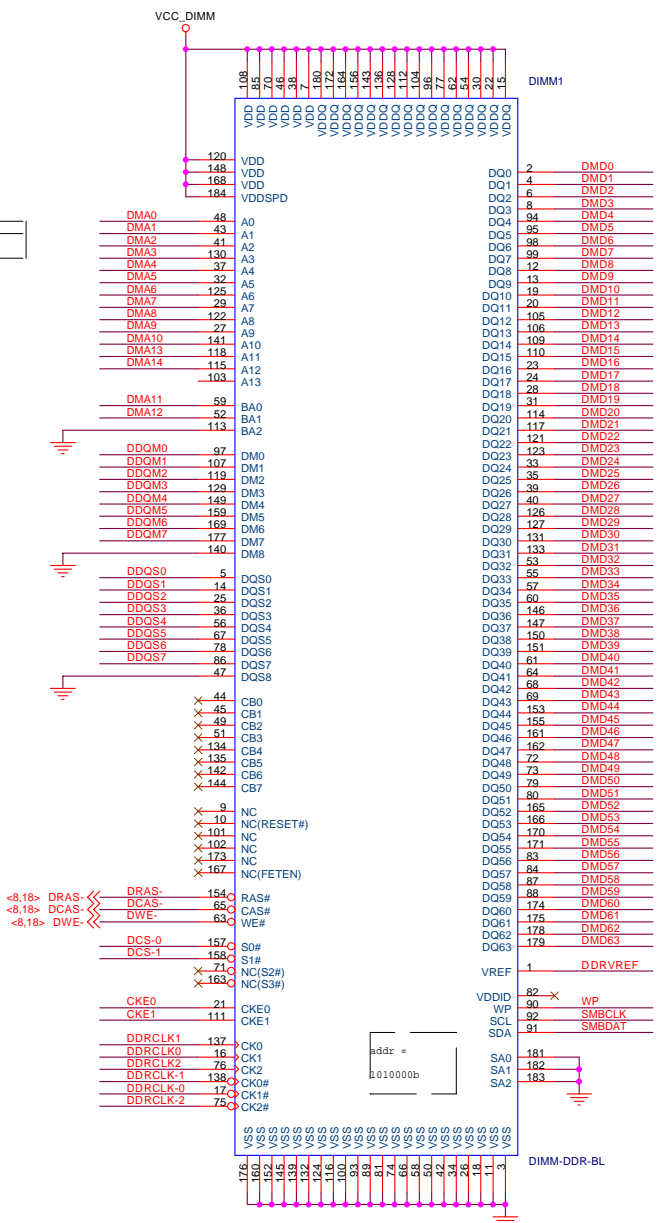


NOTE:  
VDDID IS A TRAP ON THE DIMM  
MODULE TO INDICATE:  

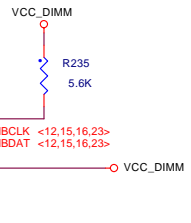
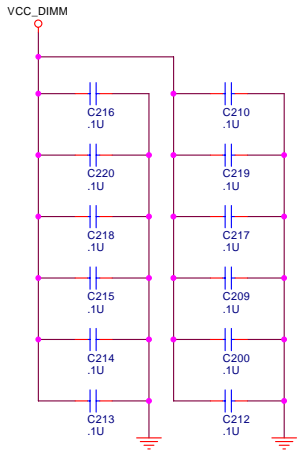
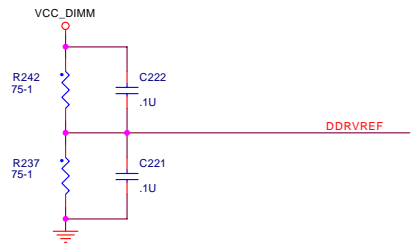
VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDDI+=VDDQ

MEMORY MUX TABLE:

SDR	DD
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7



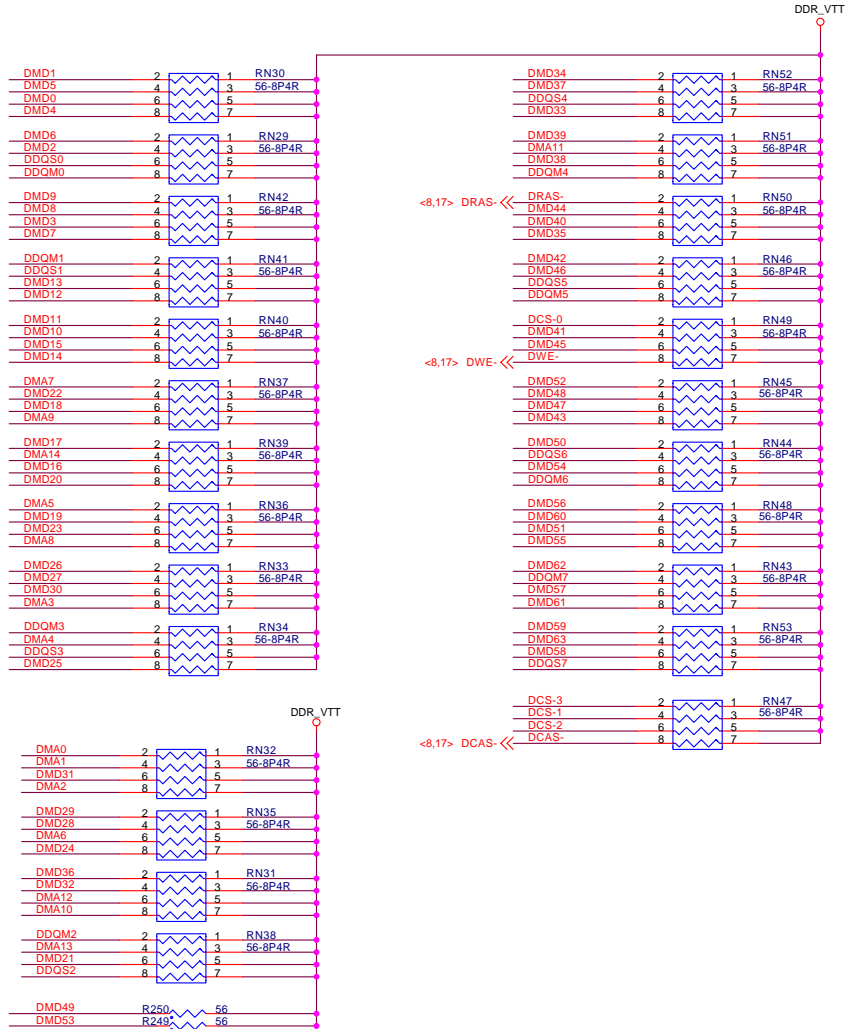
- DMD[0..63] <<DMD[0..63] <8,18>
- DMA[0..14] <<DMA[0..14] <8,18>
- DDQM[0..7] <<DDQM[0..7] <8,18>
- DDQS[0..7] <<DDQS[0..7] <8,18>
- DCS[0..3] <<DCS[0..3] <8,18>
- CKE[0..3] <<CKE[0..3] <8>
- DDRCLK[0..5] <<DDRCLK[0..5] <16>
- DDRCLK[0..5] <<DDRCLK[0..5] <16>



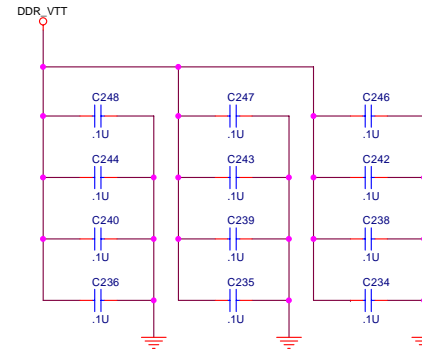
# SSTL-2 Termination Resistors

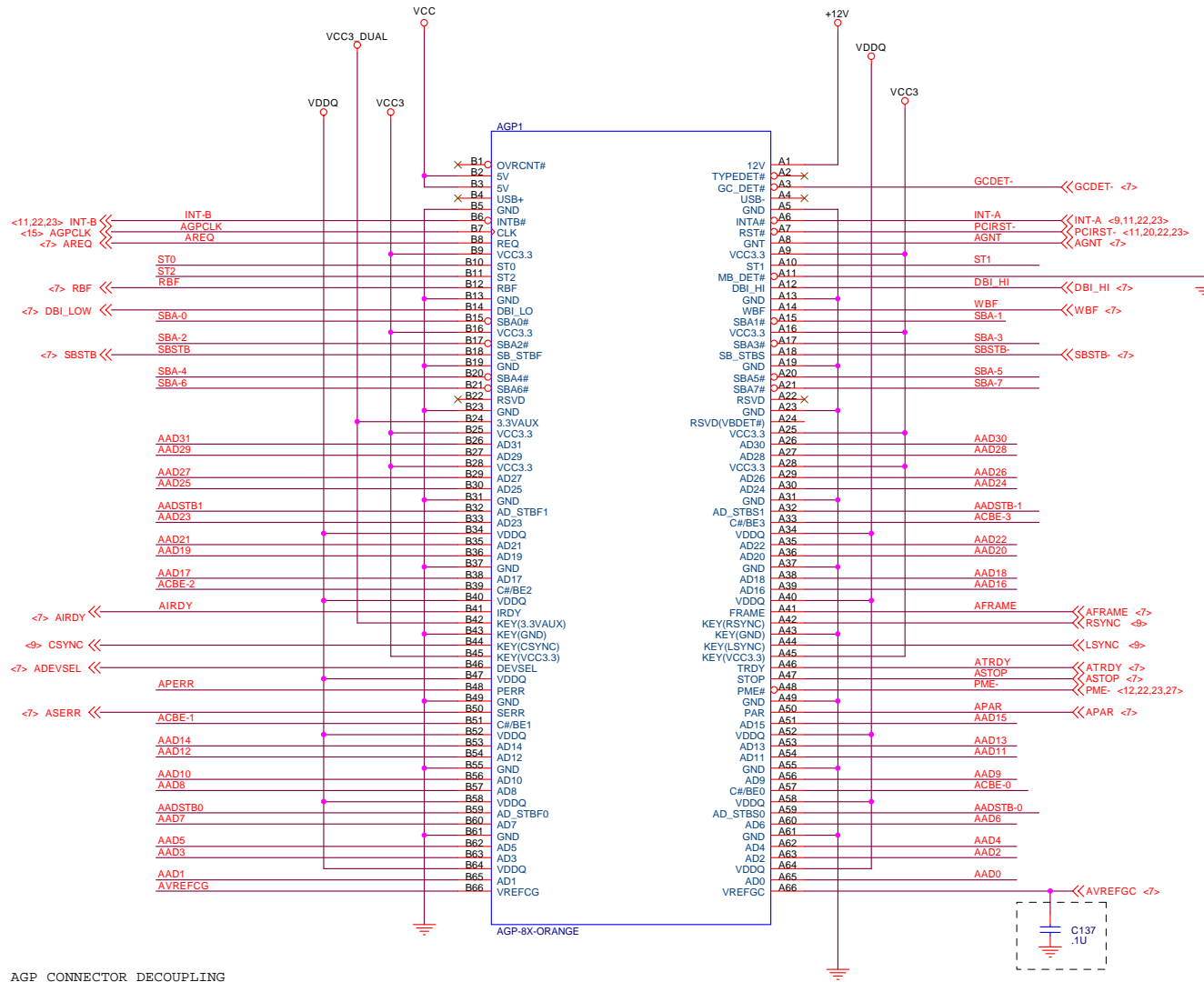
MD/DQM (/DQS)	LV-CMOS	Ra	0/10/-	DDR	Ra	Rtt
MA/Control	LV-CMOS		10	SSTL-2	10	33
CS	LV-CMOS		0	SSTL-2	0	47
CKE	0D 3.3V			DD 2.5V		

DMD[0..63]	<<DMD[0..63] <8,17>
DMA[0..14]	<<DMA[0..14] <8,17>
DDQM[0..7]	<<DDQM[0..7] <8,17>
DDQS[0..7]	<<DDQS[0..7] <8,17>
DCS-[0..3]	<<DCS-[0..3] <8,17>



**DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND**  
**0603 Package placed within 200mils of VTT Termination R-packs**





<7> SBA[0..7] << SBA[0..7]

<7> ST[0..2] << ST[0..2]

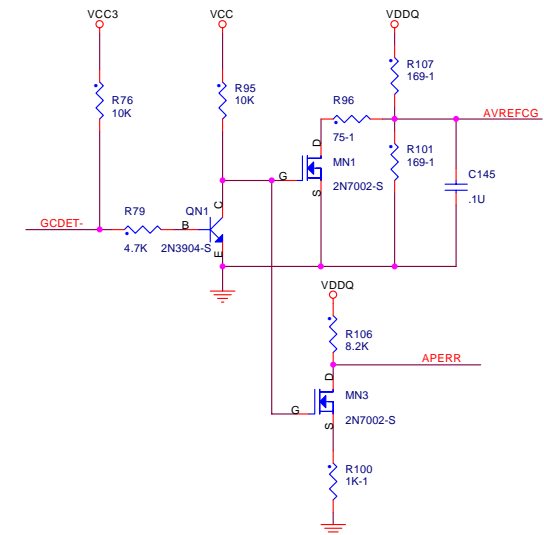
<7> ACBE[0..3] << ACBE[0..3]

<7> AAD[0..31] << AAD[0..31]

<7> AADSTB[0..1] << AADSTB[0..1]

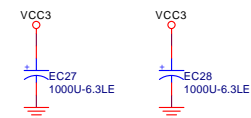
<7> AADSTB[0..1] << AADSTB[0..1]

GCDET-	Low	Hi
Graphic Card	AGP 3.0	AGP 2.0
AVREFCG	0.35	0.75
APERR	0	1.5

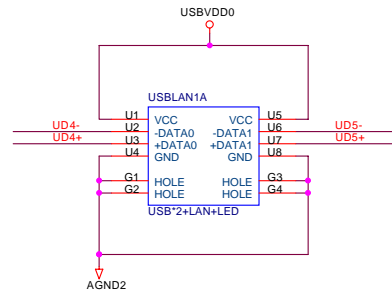
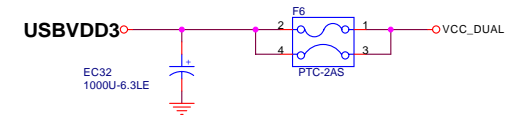
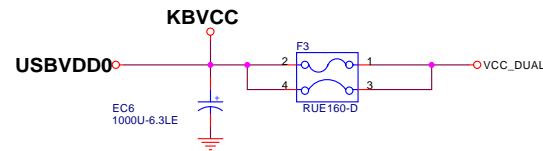


# AGP CONNECTOR DECOUPLING

put CAP close to AGP slot each POWER PIN

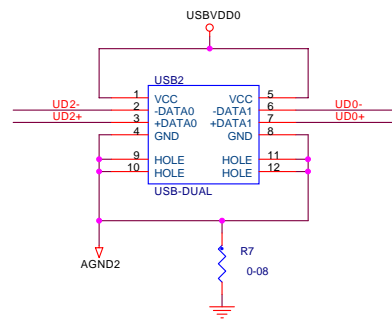






UD5- <<UV5- <13>  
UD5+ <<UV5+ <13>  
UD4- <<UV4- <13>  
UD4+ <<UV4+ <13>

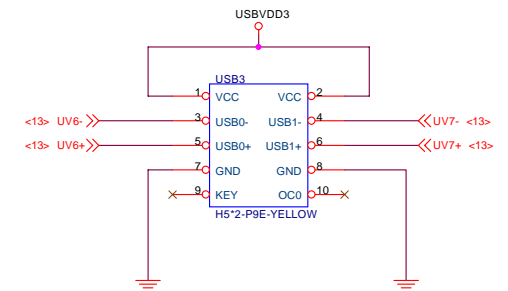
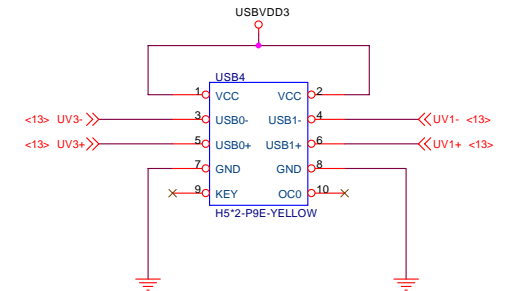
Close to USBLAN1 connector



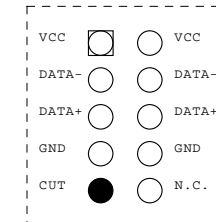
UD0- <<UV0- <13>  
UD0+ <<UV0+ <13>  
UD2- <<UV2- <13>  
UD2+ <<UV2+ <13>

Close to USB1394A\_J1 connector

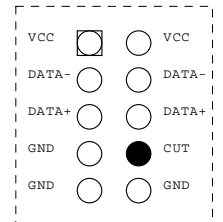
	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5



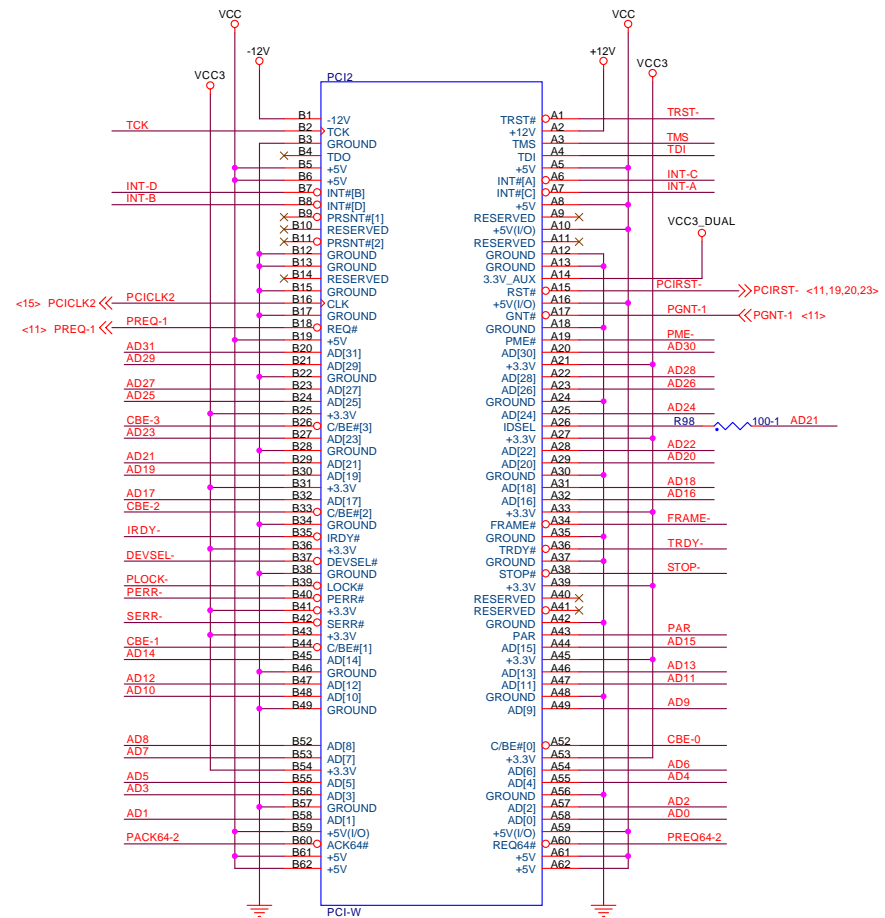
#### Intel USB Header



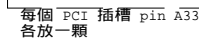
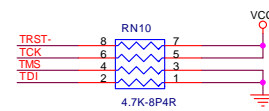
#### ACER USB Header

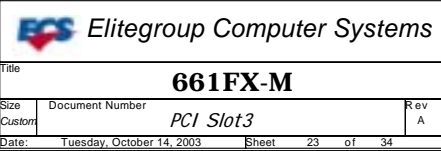


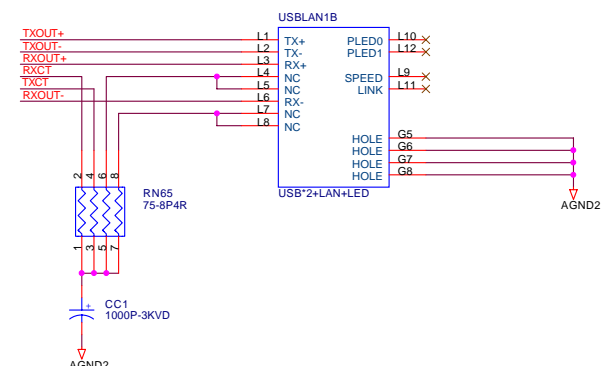
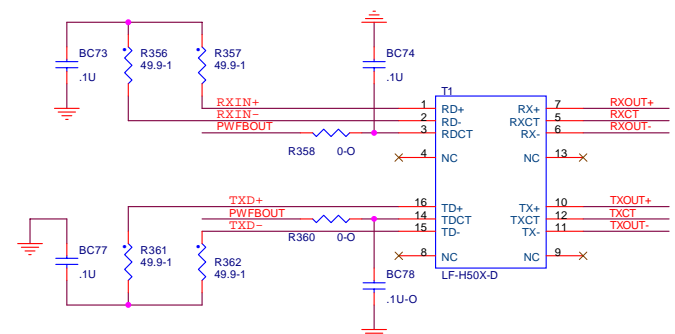
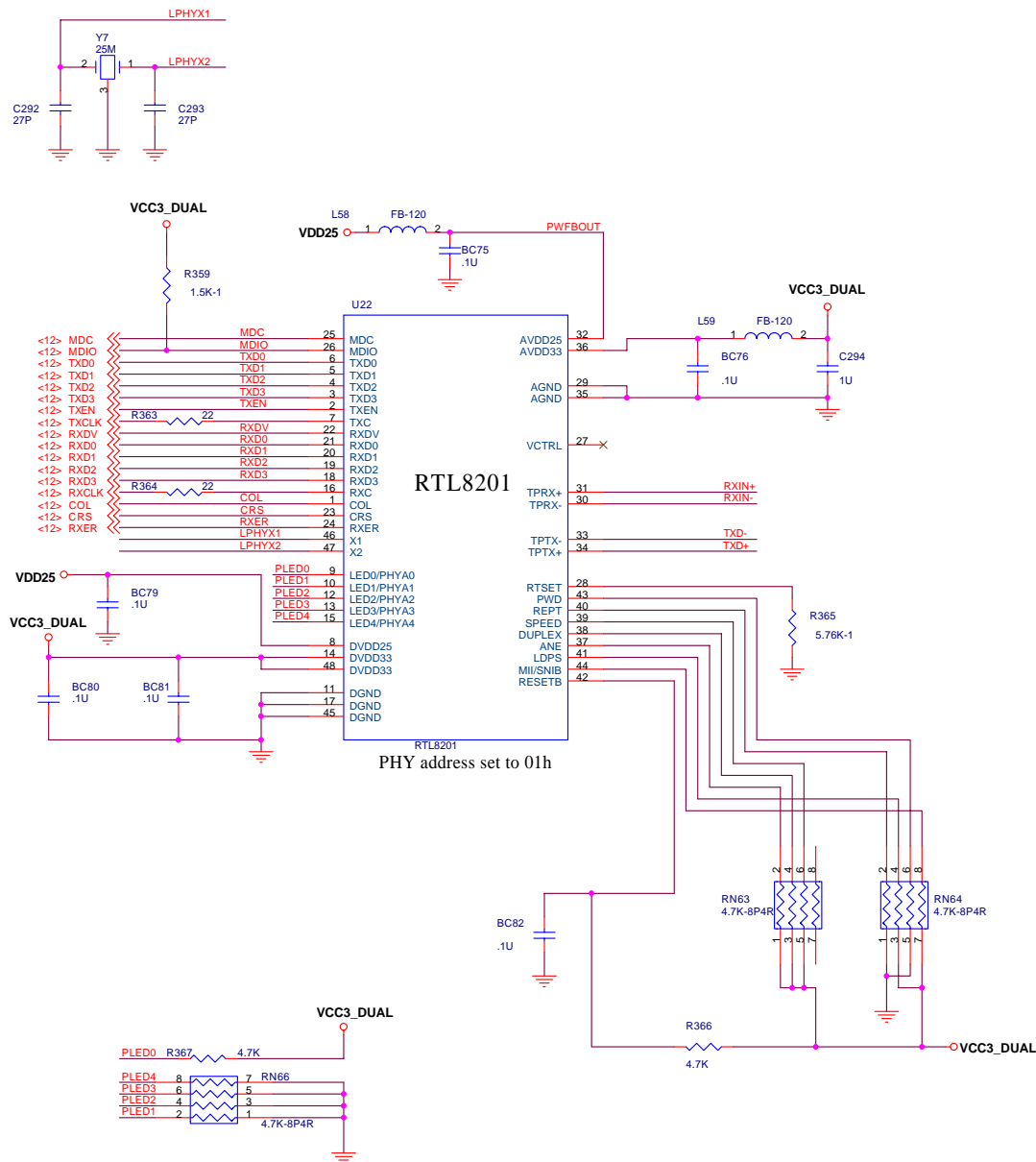
<11,23> CBE-[0..3] << CBE-[0..3]  
<11,23> AD[0..31] << AD[0..31]



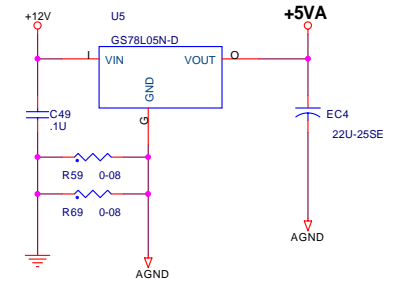
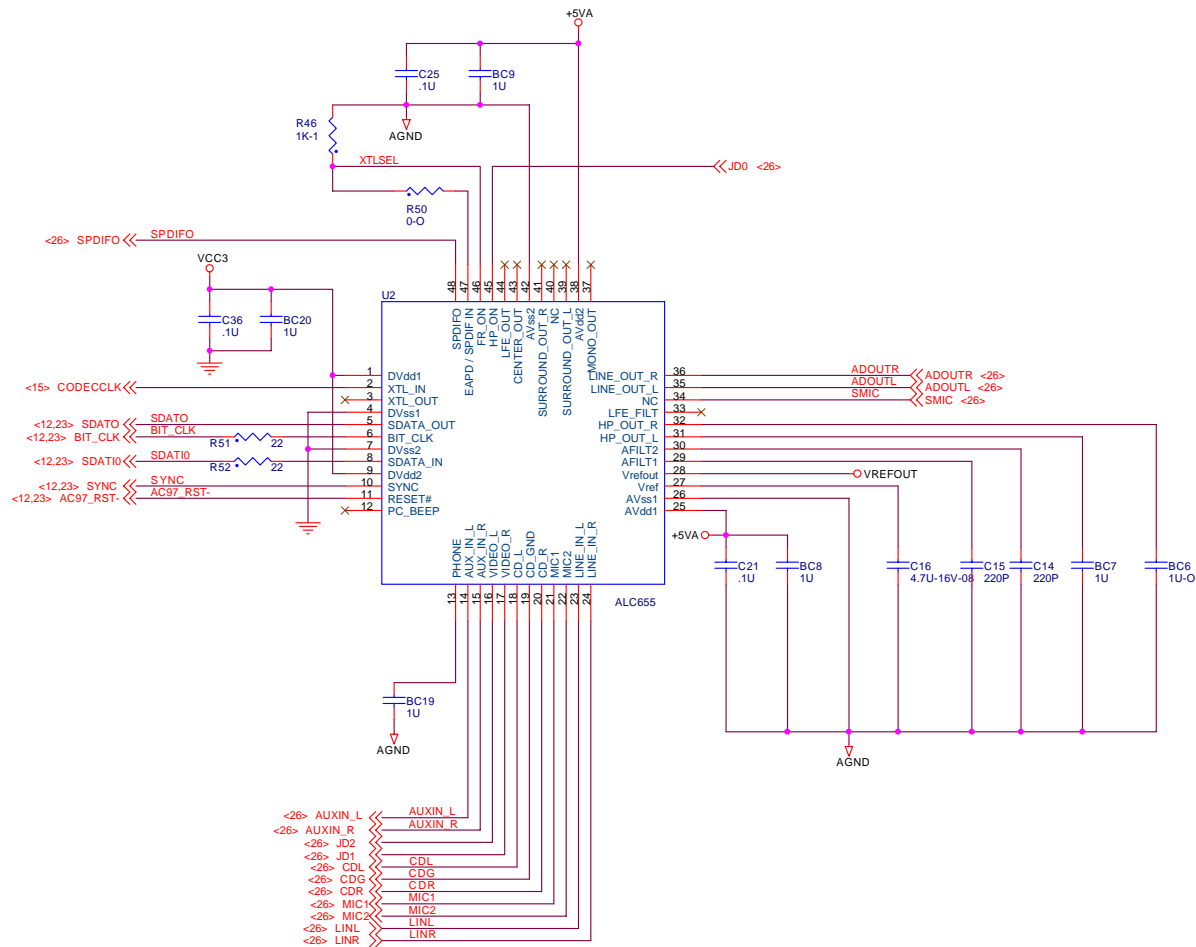
```
IDSEL=AD21
INT[C,D,A,B]
```

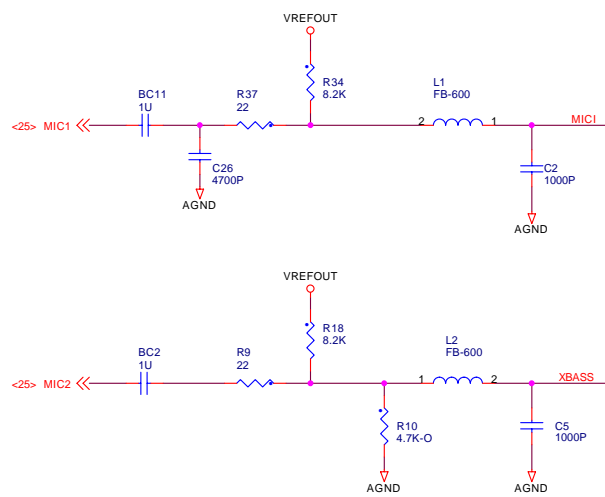
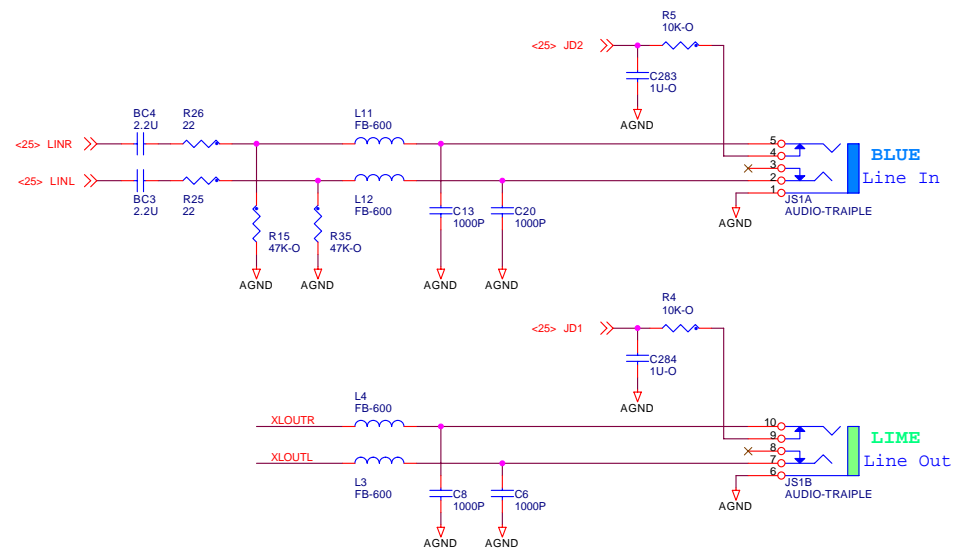
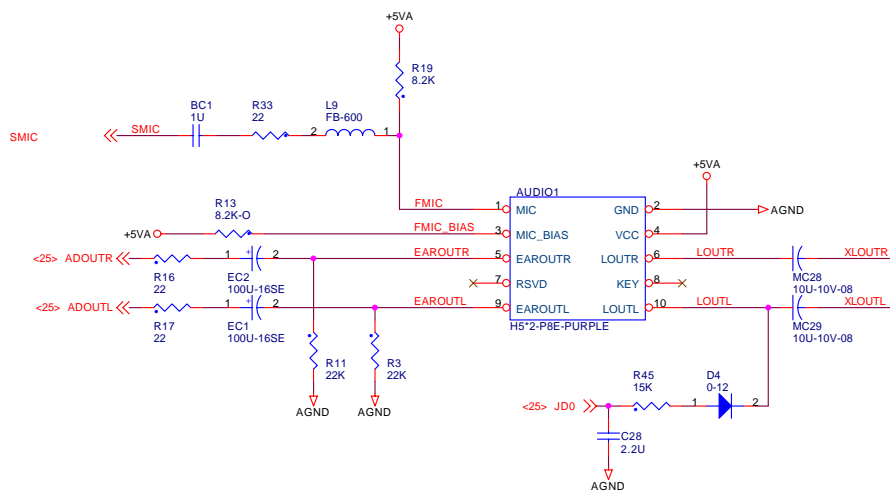




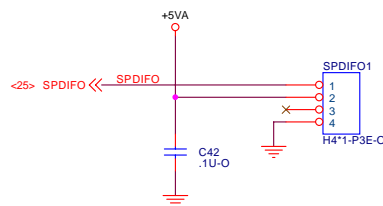
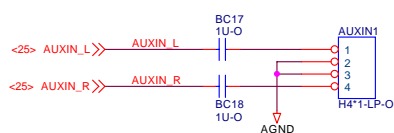
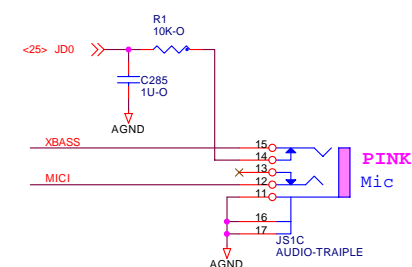
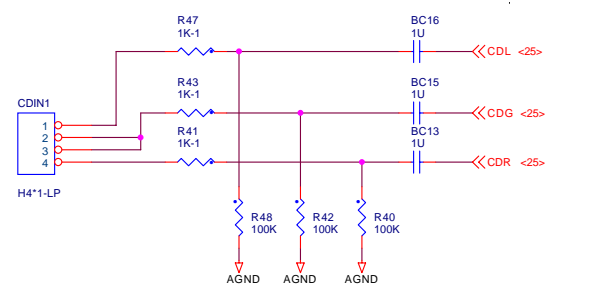


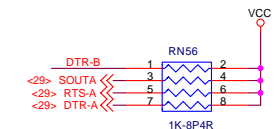
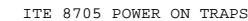




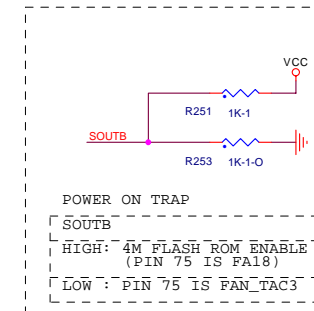


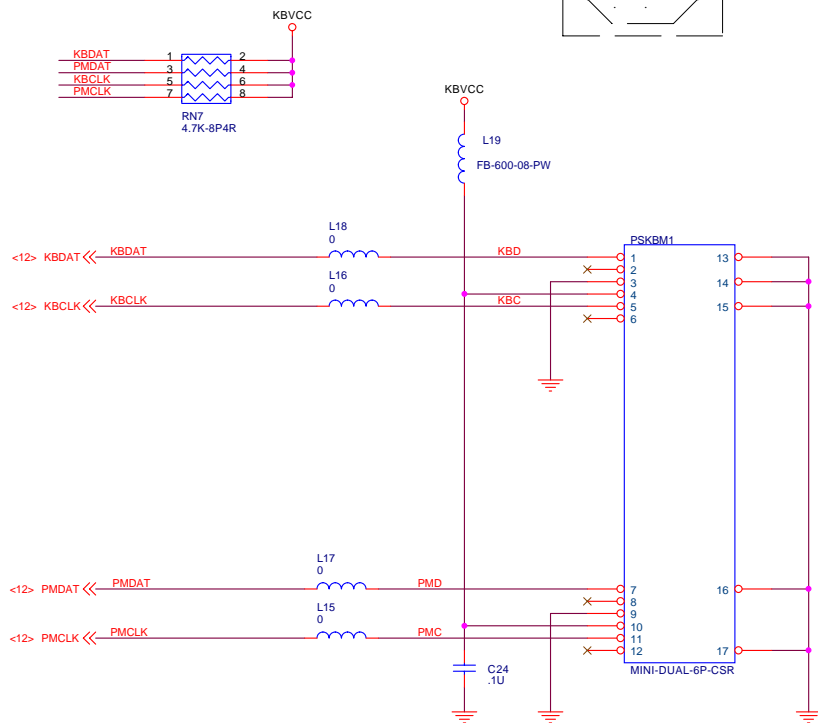
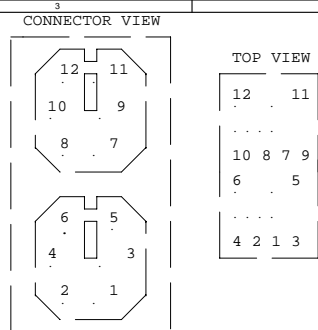
CD-IN



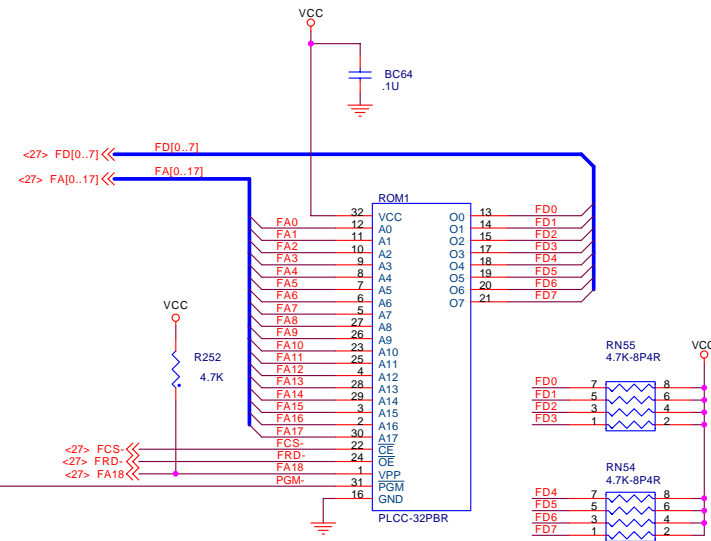


- 1.If use LPC ROM, pull down  
DTR#A RTS#A SOUTA DTR#B
- 2.If use Legacy 2MB flash rom, pull high  
DTR#A RTS#A SOUTA DTR#B
- 3.If use Legacy 4MB flash rom, pull high  
DTR#A RTS#A SOUTA DTR#B SOUTB

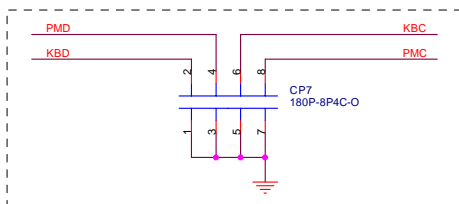


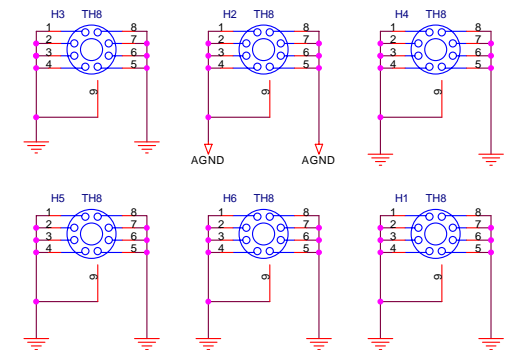
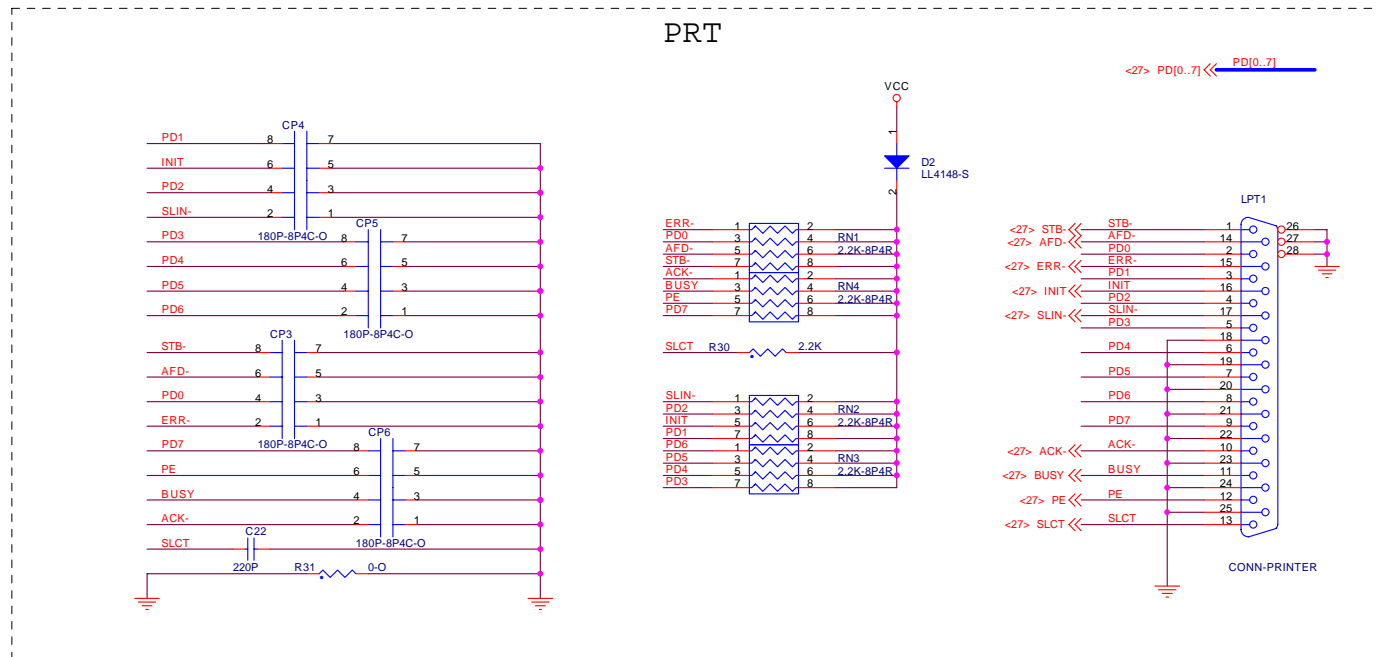
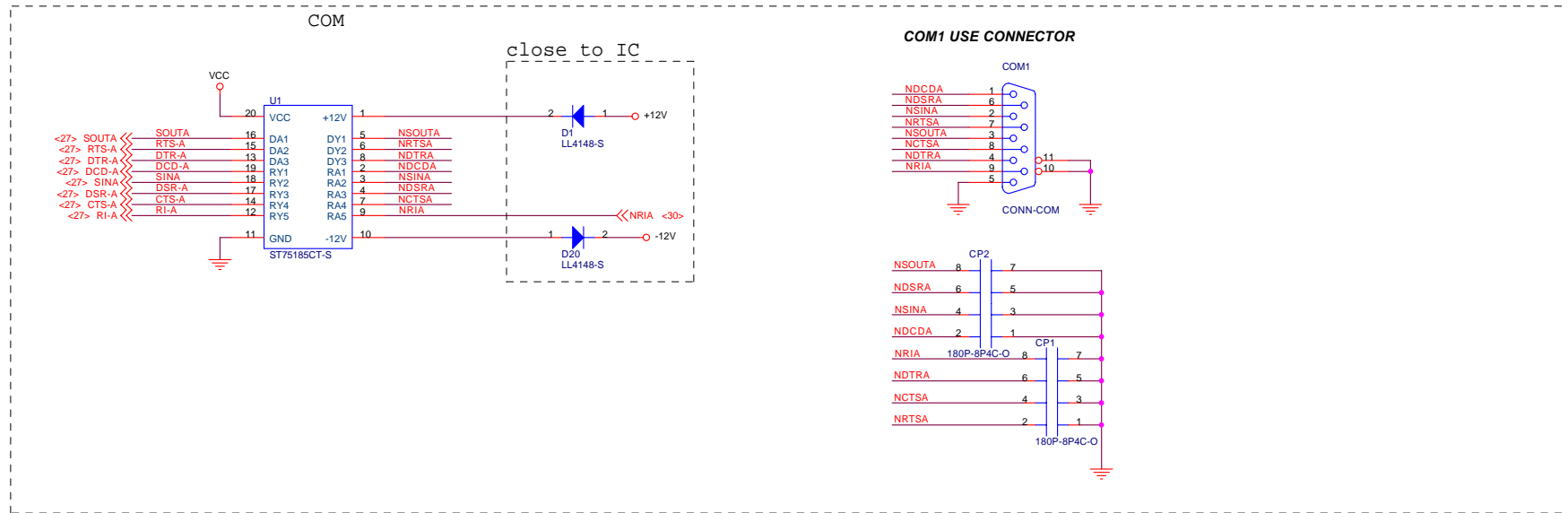


JP3	BIOS PROTECT
1-2	Write Enable
2-3	Write Disable

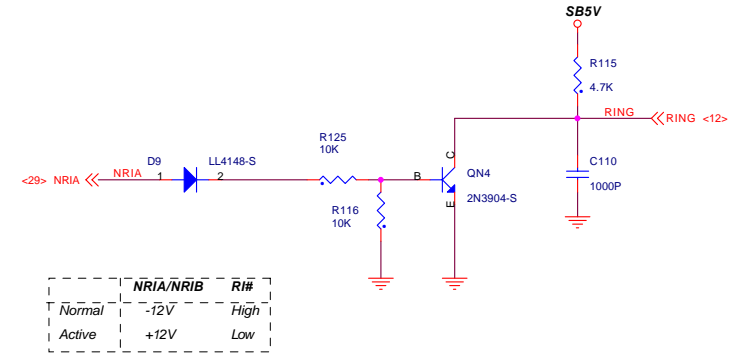
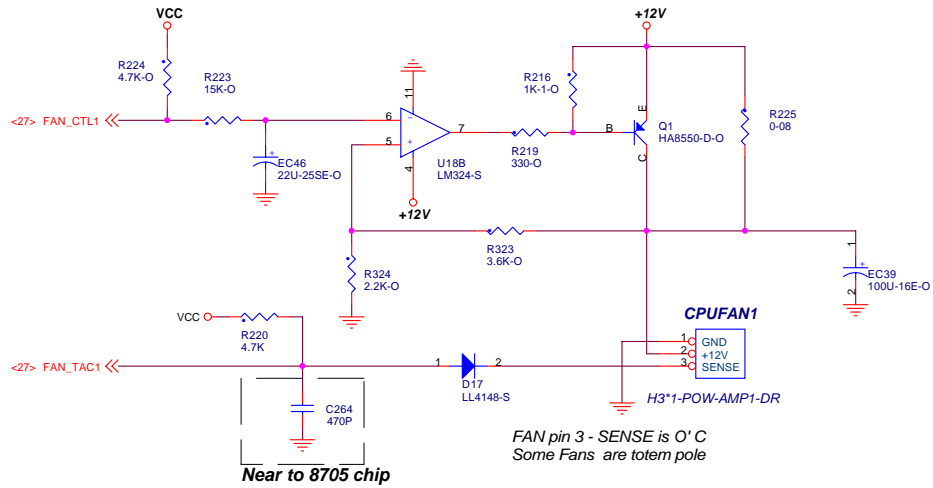


PLACE NEAR CONNECTOR



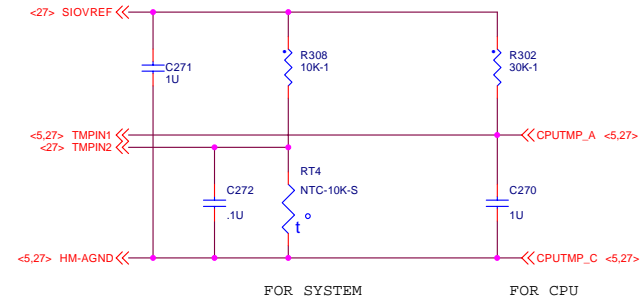


**Layout :**  
Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA .

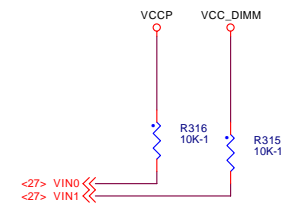


## Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode

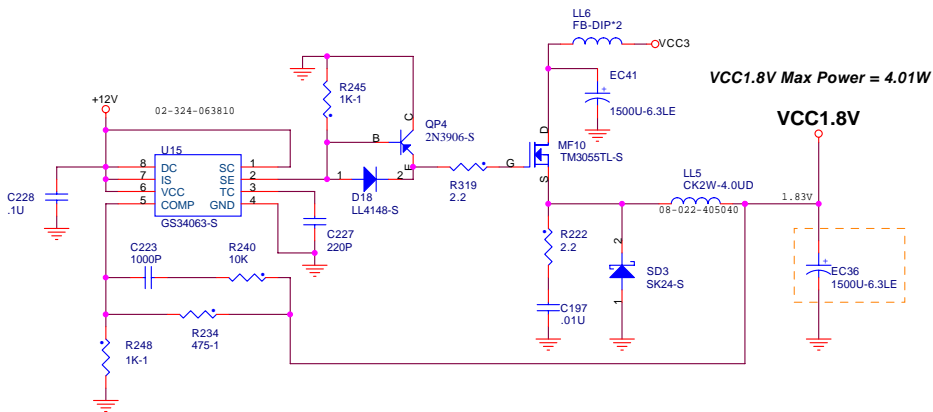


## Voltage Monitor



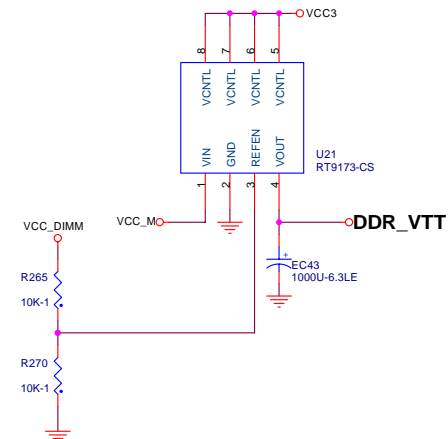
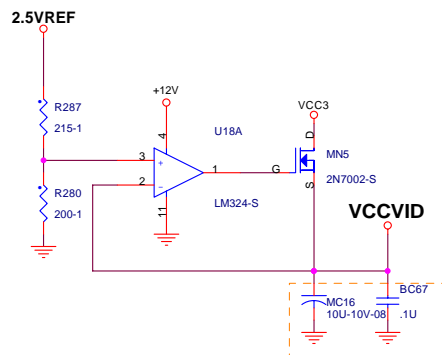
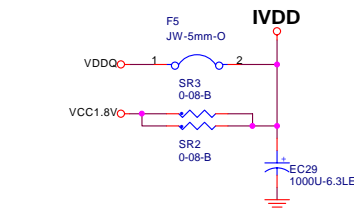
**Elitegroup Computer Systems**

Title			<b>661FX-M</b>
Size	Document Number	HM / FAN / RING	
Custom		Rev	A
Date:	Tuesday, October 14, 2003	Sheet	30 of 34

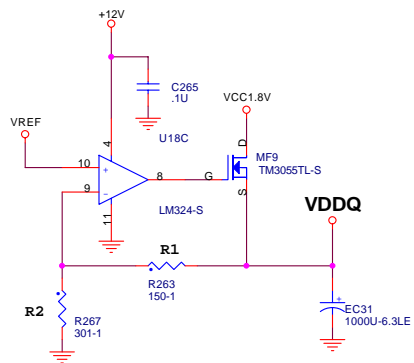


	IVDD	VCC1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator or two regulator
661FXLV	1.5V	1.8V	two regulator

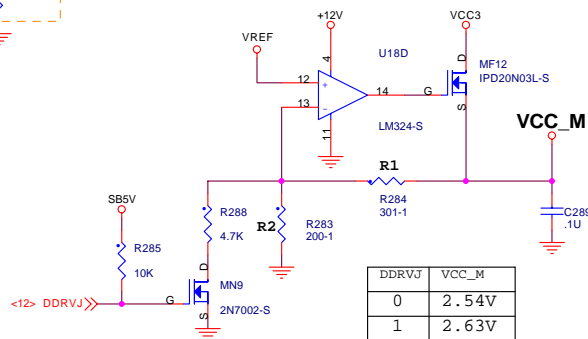
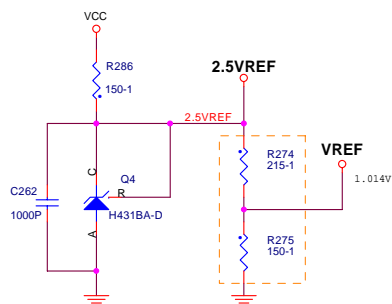
	AUX_IVDD	SB1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator
661FXLV	1.5V	1.8V	two regulator



VCC1.5V Max Power = 0.3\*(0.289+2.35)=0.7917W



$$V_o = V_{REF} (1 + R_1/R_2)$$



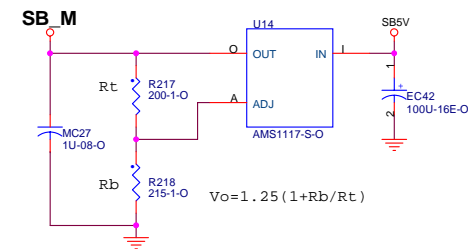
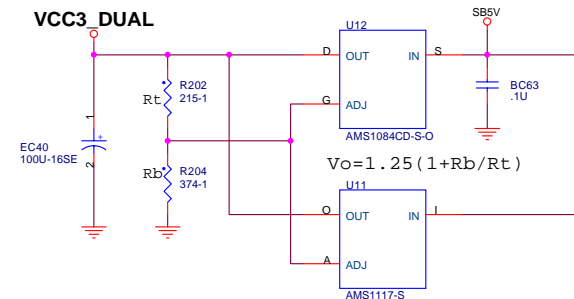
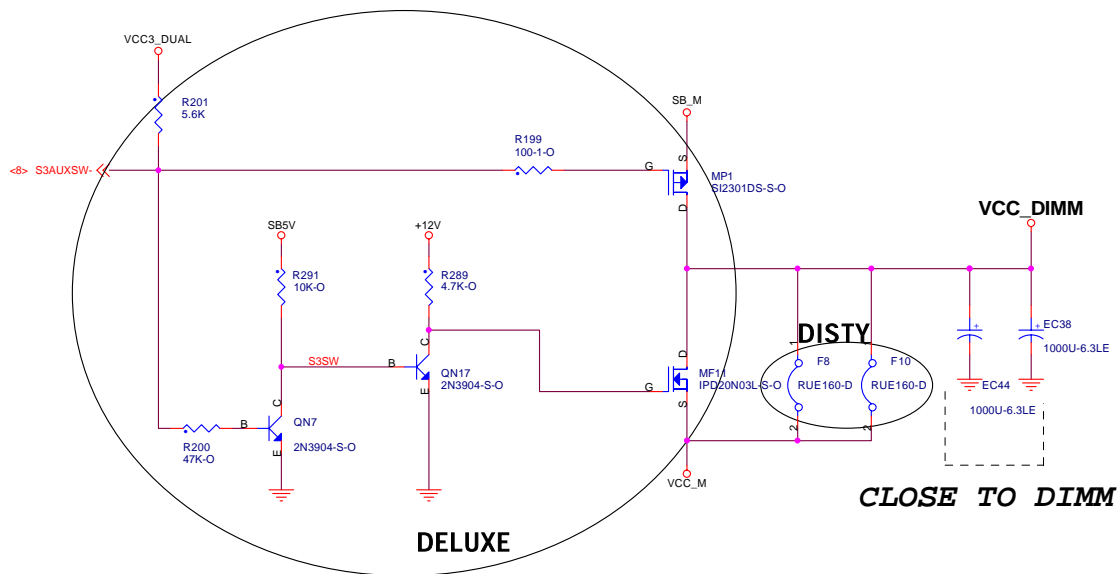
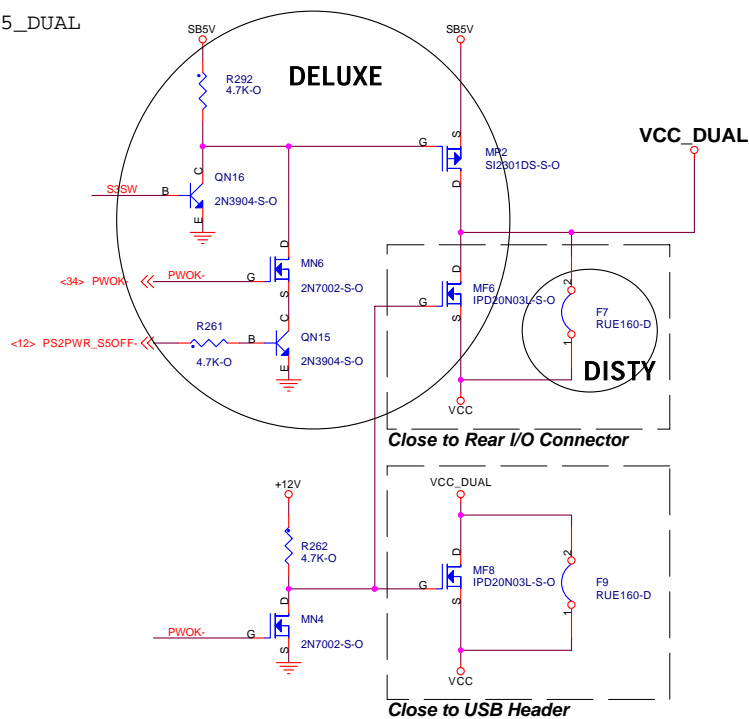
DDRVJ	VCC_M
0	2.54V
1	2.63V

```
1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER
```

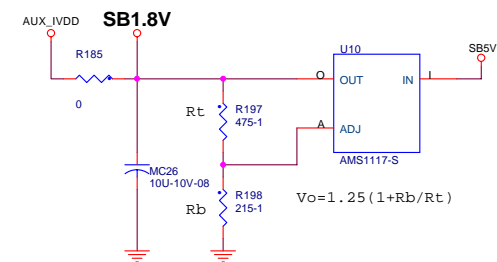
2.IN S3,S4,S5  
THIS CIRCUIT PASSES THE STANDBY POWER

NOTE:  
BECAUSE OF THE MAXIMUM CURRENT FROM  
POWER SUPPLY IS ONLY ABOUT 750-1000mA  
SO IF YOU WANT TO SUPPORT WAKE UP  
FROM S3 BY USB, YOU MUST HAVE A POWER  
SUPPLY WITH LARGER POWER.(ADDITIONAL  
500mA PER USB PORT)

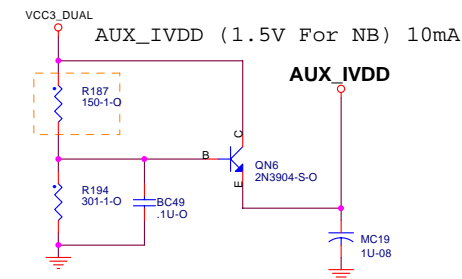
VCC3\_DUAL & VCC5\_DUAL



SB1.8V (For SB) 450mA



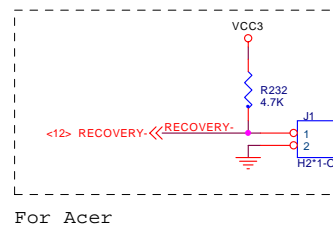
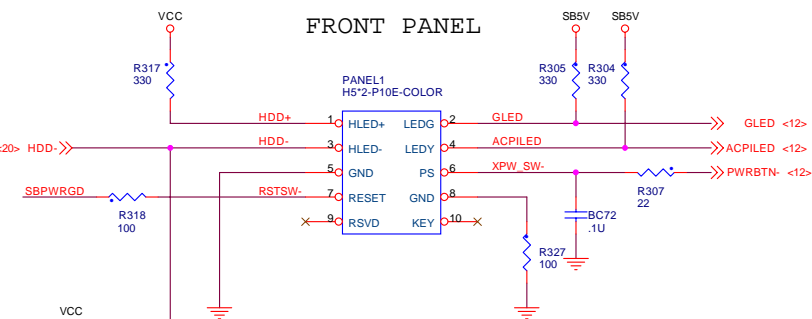
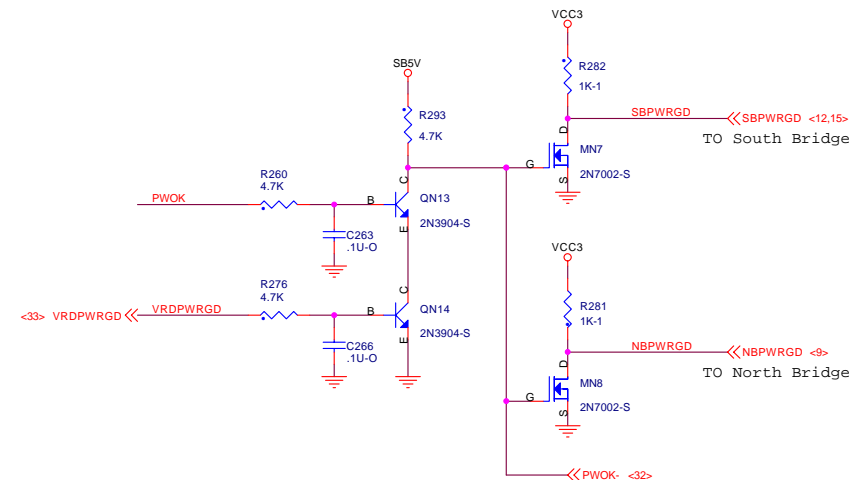
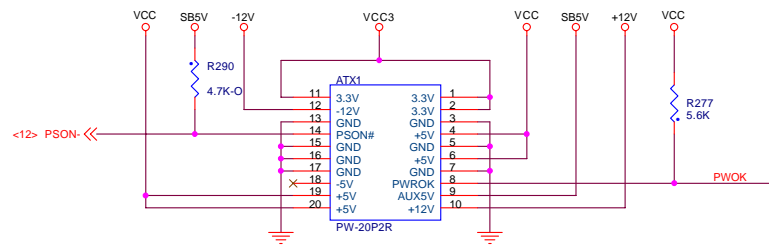
AUX\_IVDD (1.5V For NB) 10mA



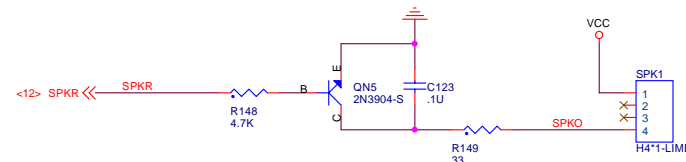
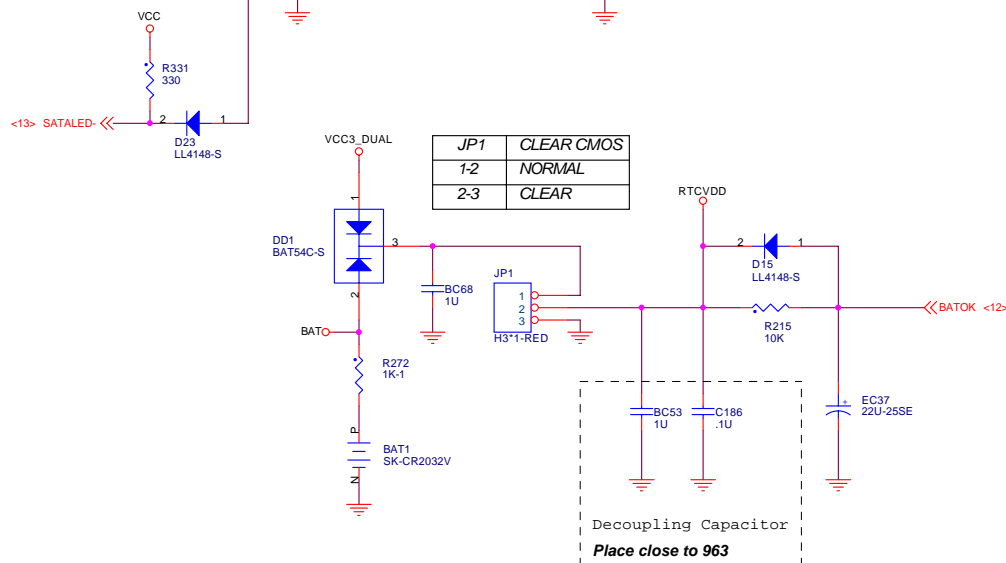
Title		<b>661FX-M</b>	
Size Custom	Document Number	<i>Dual 5V&amp;3V, STR</i>	Rev A
Date:	Monday, December 08, 2003	Sheet	32 of 34







For Acer



RTC

NOTE!

- 1.The RTCVDD is 3V
  - 2.Decoupling capacitor must be close to 635 RTCVDD pin.
  - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.